Sci.Int.(Lahore),28(4),4141-4147,2016 ISSN 1013-5316;CODEN: SINTE 8

DESIGN OF ZETA CONVERTOR WITH IMPROVED POWER QUALITY FOR BRUSHLESS DC DRIVES

Usama Baig[1], Muhammad Amjad[2], Kamran Maqsood[3]

University College of Engineering and Technology (UCE&T)
The Islamia University of Bahawalpur, Pakistan
Correspondance: mirzausamabaig12@gmail.com

ABSTRACT: *Development of a quality improved zeta converter feeding brushless DC (BLDC) drives.1-θ AC, rectified using diode bridge rectification (DBR) and a discontinuous current interval in an inductor of zeta converter in front of inverter is studied in this paper. The zeta work as a pre regulator when it is operating in discontinuous inductor current interval. In this scheme only one sensor used to control voltage of zeta converter for the large range of speed control of the brushless DC drive. This topology enables the switching of voltage source invertor on fundamental frequency to minimize the switching losses. The suggested scheme for the Brushless DC drive is developed and its operation and results are observed in MATLAB for attaining the improved power factor for the large range speed control. The achieved results are in the allowable limits of worldwide power criteria.*

I. INTRODUCTION

Brush less DC drive has gained much attention in past decade due to wide range of speed, less Electromagnetic interference (EMI), high ruggedness, high flux density, comparatively high efficiency, and minimize the maintenance requirements [1]. Aforementioned properties grapes the attention from wide areas like aerospace, industrial tools, hybrid automation, in robots like actuators and position sensors, home and industry ventilation, power plants and other household applications. 3-phase BLDC motor generally encompasses of 3-phase stator winding and PM (Permanent Magnet) rotor which makes it synchronous. As name suggest that it consist on PM rotor and brush less commutator which rejects the sparking, overheating, brush losses, low Electromagnetic Interference (EMI) and maintenance cost. It having same torque speed characteristics as of typically used DC motors. The commutation assembly works electronically and so called electronic commutation assembly which based on Hall Effect. Rotor speed positioning measured at 60 degree used to feed the current into stator winding via Voltage Source Invertor (VSI) [2]. Typically speed control of BLDC motor established on PWM (Pulse Width Modulation) is used. The PF (Power Factor) disturbance occurred due to Capacitor as it draws 70-80% of current supplied with THD (Total harmonic Distortion) which lead to exceed the international power quality criteria (IEC 6100-3-2) [3]. In previous decade many researchers have suggested different approaches for power factor correction convertors of BLDC motors. The suggested converters typically operate in both intervals (Continues Conduction Interval) CCM and Discontinues Conduction Interval (DCM). There is tradeoff between stress on converter and power rating depends on interval of operation.

For class A application (<16 A, <600 W) for mainly household applications high PF (Power Factor) and low THD is required according to international power quality standards. According to pervious literature the power quality improvement obtained using conventional boost PFC AC-DC convertor [4]. In which a constant DC link voltage is maintained at feed of VSI and PWM based current control is used for speed control. There is tradeoff between high switching frequencies (9-20 kHz) of invertor and switching losses as a high switching frequency normally increases the switching losses. Madani, S.M. [5] has been suggested four switch configuration with low cost with trade of as extra PWM switching of all switches at VSI which leads to high switching losses.

The active rectifier configuration in front of VSI for BLDC drive has been suggested in [6]. This model requires higher number of sensors resulting higher cost and complicated control.

Singh, S. [7] has been suggested similar model with front end Cuk convertor for PFC of BLDC motor. This method is use CCM (Continues Conduction Interval) of Cuk convertor which control voltage at DC-link and control PFC of high power drives.

BC (Bridgeless Configuration) of SEPIC and buck-boost converters has been suggested in [8]. Advantages of the suggested model is in terms of reduced losses and the disadvantage is the cost in terms of large number of required active and passive elements.

4142 ISSN 1013-5316;CODEN: SINTE 8 Sci.Int.(Lahore),28(4),4141-4147,2016

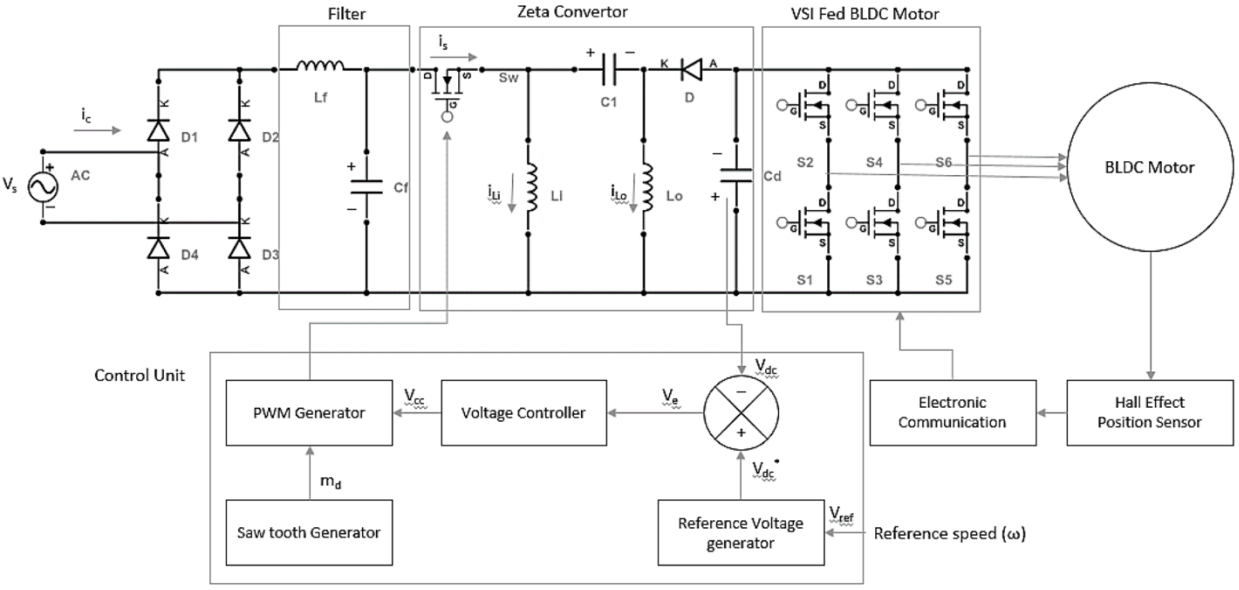

Fig 1 Model for PFC Zeta DC Motor Convertor Fed Brushless DC Motor

A Zeta Convertor PF pre-regulator has been widely used and it has gained reputation due to its quick dynamic performance and relatively better with light load circumstances [9]. It operates in CCM that requires a three sensor with two control loop which is costly and recommended for high power applications.

A altered Zeta convertor as PF regulator is , and its applications for low cost BLDC drive is investigated in this paper.

II. Anticipated Zeta Convertor fed BLDC drive

The suggested zeta convertor arrangement follows invertor in front of BLDC drive is displayed in Fig 1.

The controlled DC voltage of invertor is used to control the speed of BLDC drive. The pre-regulated power factor improved zeta convertor is intended to work in DICM (discontinuous inductor current interval). The voltage follower method is used for PFC Zeta convertor to operate in DCIM which requires only one sensor for the control of DC voltage. Thus the switching of invertor for electronic commutation is on fundamental frequency that offers the reduction of losses in VSI. The suggested model for zeta convertor is designed and simulated in Matlab for enhanced power factor for extensive range of speed control. The results of suggested drive are observed for different supply voltages and it's obtain power factor is acceptable under IEC 61000-3-2.

III. Suggested Zeta converter operation

The suggested model is designed to work in discontinuous inductor conduction interval such that there is discontinuity in conduction of output inductor Lo in a complete cycle. Four intervals of conduction (A, B, C, D) are displayed in fig 1.

A. Interval A

Interval A operation is displayed in fig 2, when the switch S_w is turned on, current passed through the energy storing elements and so energy stored in inductors (L_i, L_o) and capacitor (C_1). Storing in energy raised the currents in respec inductivetors (L_i, L_o) and raised voltages across

Capacitor (C_1). As displayed in fig 2, the midway capacitor C_1 is charged in negative direction whereas diode D is turned

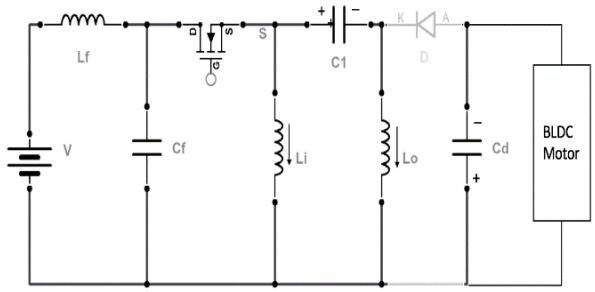

Fig 2 Interval A

off

and the Capacitor C_d delivers energy to the load. As the Capacitor releases its energy, voltages across C_d also decreases.

Second interval of interval A operation is just similar to previous operation with inverse polarity of midway capacitor C_1. When the switch S_w is turned on, currents i_{Li} , i_{Lo} and voltages across the midway capacitor C_1 increasing continuously. With respect to corresponding duty cycle, Interval A complete operation constitutes 15 to 25% of switching time period.

Sci.Int.(Lahore),28(4),4141-4147,2016 ISSN 1013-5316;CODEN: SINTE 8

C. Interval B

In this interval when switch S_w is turned off, discharging path for C_1 through diode D is turned on so midway capacitor C_1 start to discharge whereas the Capacitor C_d now start to charge through diode D. voltages across C_d and current through L_i increases whereas voltage across C_1 and current through L_o decreases. Direction of currents and polarities of voltages are displayed in fig 3. Change the current and voltages in interval B. Current passing through diode D is equal to sum of total currents passing through inductors (L_i and L_o). Discharging of midway capacitor C_1 and charging of capacitor C_d becomes to end when both the capacitors maintain equal potential such that diode D_1 becomes open

D. Interval C

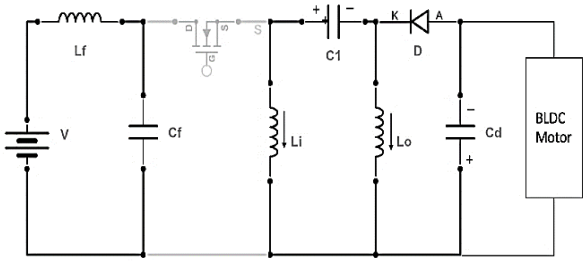

Fig 3 Interval B

In this interval the voltages across the capacitor C_1 becomes less than the voltage across capacitor C_d which turns on the diode D. With short of discharging path, midway capacitor C_1 discharges through inductor L_i and L_o as displayed in fig 4. Inductor L_o discharges continuously to Capacitor through diode D. Due to discharging the value of current through inductor L_o decreases continuously also the current of inductor L_i increases in interval C. This interval of operation ends as the current of output inductor L_o come to be zero.

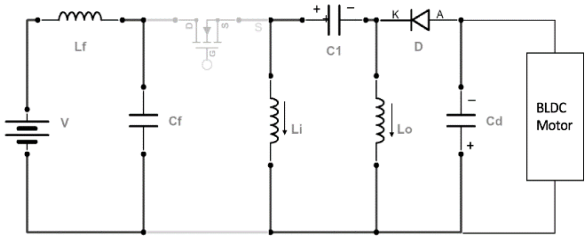

Fig 4 Interval C

E. Interval D

For the interval of discontinuous conduction, the parameters designed for both inductors are different such that Li is much higher as compared to L_o which guarantees the discontinuous operation interval in mentioned settings so L_o discharges completely in a cycle. In this interval of operation, the midway capacitor discharges continuously so that voltages across C_1 decreases whereas the current through L_i increases continuously. The diode D remain turned off and the current through Lo becomes equal to the current through L_i in this interval. During this operation the Capacitor C_d supplies the energy to drive and operation becomes to end when C_1 discharged completely.

The second interval of operation in its parental interval D is next step of aforementioned operation when C_1 becomes fully discharged it starts charging again in opposite direction. For charging operation, the current is supplied through inductor L_i and the capacitor C_1 charged to its value. With the charging of C_1 the voltages across C_1 increases continuously whereas the current through L_i decreases with increase of V_{dc} as displayed in fig 3. The diode D continue in its off

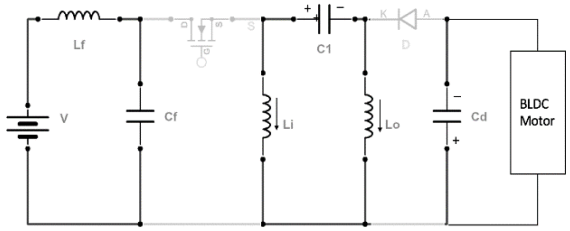

Fig 5 Interval D

conduction interval and the capacitor C_d supplies energy to the output drive. The operation interval D constitutes 50 to 70% time of complete switching period. Complete interval D operation is displayed in fig 5.

IV. Design of improved zeta converter

For the operation of suggested converter, the ideal selection inductors (L_i and L_o), centered and capacitors (C_1 and C_d) the inductor and capacitor for DC filter (C_f and L_f) are necessary for required action. Some assumption are made for the suggested converter are as follow:

1) The PFC converter has ideal components such that there is no loss output and input powers are equal.
2) The resistance of inductor are assumed to be zero such that there is no saturation in the inductors.
3) Midway and capacitor C_d are supposed to be ideal such that they have zero equal resistance.
4) The switching periods are considered to be zero as relative to time constant of capacitors and inductor.

The converter have to work in DCIM so that current through inductor come to be discontinuous in all switching duration. The DC link voltage are controlled by PI controller such that V_{dcmx}=200V and V_{dcmn}=50V. For the worse case of duty cycle in which supply voltage is minimum inductor is designed to operate in discontinuous interval. The power factor convertor in designed for 350W BLDC motor.

$$V_{supply} = V_{max}(2\pi f_L t) = 220\sqrt{2}\sin(314t)\,V \qquad (1)$$

Peak input voltage V_m and f_L is 50 Hz the line frequency.

The instantaneous voltage across DBR is given as

$$V_i(t) = |V_{max}\sin\omega t| = \left|220\sqrt{2}\sin(314t)\right|V \qquad (2)$$

The buck boost configuration of zeta converter are as

$$V_{dc} = \frac{D}{1-D}V_i(t) \qquad (3)$$

Where D is duty ratio, its depend on the input DBR voltage and Capacitor voltage The value of duty cycle is obtained by substituting and rearranging equation (2) and (3) as

$$D(t) = \frac{V_{dc}}{V_i(t) + V_{dc}} = \frac{V_{dc}}{V_m \sin \omega t + V_{dc}} \quad (4)$$

The P_i power transmitted and the DC voltage as the function of V_s as the speed of BLDC drive is controlled by changing the DC voltage fed to the invertor, since the Ri of converter is give as

$$R_{in} = \frac{\{V_{in}(t)\}^2}{P_i} = \frac{V_s^2}{p_i} \quad (5)$$

Therefore the R_{in} value depend upon the DC link voltage and supply voltage.

For the rated power P_{max} =350W and the supply voltage the V_s=85v the value of R_{in} is 20.64Ω and the maximum value as the V_{dc} 50V and Power 87.5W with V_s=270V is 1041.43 Ω. Hence the R_{in} varies from 20.64Ω to 1041.43 Ω.

A. Design of inductor L_i

The η is the current ripple allowed by inductor, at the rated conditions V_{dc}=200V and the minimum value of Vs maximum current is obtained, hence the L_i is designed for minimum value of Vs as [10].

$$L_i = \frac{1}{\eta f_s}\left(\frac{V_{s\,mn}^2}{P_{mx}}\right)\left(\frac{V_{dc\,mx}}{\sqrt{2}V_{s\,mn} + V_{dc}}\right) \quad (6)$$

$$= \frac{1}{0.2 \times 20000}\left(\frac{85^2}{350}\right)\left(\frac{200}{85\sqrt{2} + 200}\right)$$

$$= 3.22\ mH$$

The value of L_i is $3.22\ mH$ for the 20 % amount of ripple current.

B. Design of Lo

The output inductor Lo designed as

$$L_{oc} = \frac{V_{dc}\left(1 - D(t)\right)}{2i_{Lo}(t)f_s} = \frac{V_{dc}D(t)}{2I_{in}(t)f_s} = \frac{R_{in}V_{dc}D(t)}{2V_{in}(t)f_s}$$

$$= \left(\frac{V_s^2}{P_i}\right)\frac{V_{dc}}{2V_{in}(t)f_s}\left(\frac{V_{dc}}{V_i(t) + V_{dc}}\right) \quad (7)$$

The worst case if the input voltage is V_{dc} 50V then the value of L_o as

$$= \left(\frac{V_{s\,min}^2}{P_i}\right)\frac{V_{dc\,min}}{2\sqrt{2}V_{in\,min}(t)f_s}\left(\frac{V_{dc\,min}}{\sqrt{2}\,V_{i\,min}(t) + V_{dc\,min}}\right)$$

$$= \left(\frac{85^2}{70}\right)\frac{50}{2\sqrt{2} \times 85 \times 20000}\left(\frac{50}{85\sqrt{2} + 50}\right)$$

$$= 315.3\ \mu H$$

The value of the L_o should be less than the critical value as a result the chosen value is 70 μH [5].

C. Design of C_1

The value of the midway capacitor C_1 in common conduction interval for k% ripple voltages is given as [3].

$$C_1 = \frac{V_{dc}D(t)}{kV_{C1}(t)f_sR_L}$$

$$= \frac{V_{dc}}{k\{V_{dc}+V_{in}(t)\}f_s\,(V_{dc}^2/P_i)}\left(\frac{V_{dc}}{V_i(t)+V_{dc}}\right) \quad (8)$$

$$= \frac{P_i}{Kf_s(V_{in}(t) + V_{dc})^2}$$

Therefore the maximum value of supply voltage V_s and DC link voltage V_{dc} are used for the value of midway capacitor C_1

$$= \frac{P_{max}}{Kf_s(V_{s\,mx}(t) + V_{dc\,mx})^2}$$

$$= \frac{350}{0.1 \times 20000\left(270\sqrt{2} + 200\right)^2} = 0.516\mu F$$

Where the value of K is selected as 10% of the minimum voltage on capacitor V_{c1}. Therefore the value of capacitor C_1 is selected as 0.68 μF for common interval conduction. The commonly used capacitors for this type of application must have low equivalent resistance which make them suitable for high frequency and high serge current applications.

D. Design of capacitor Cd

The value of Capacitor C_d as has suggested in [9].

$$C_d = \frac{I_{dc}}{2\omega\Delta V_{dc}} = \frac{P_i}{2\omega\delta {V_{dc}}^2} \quad (10)$$

Where $\delta$the voltage ripple and I_{dc} is is the current through cd, therefore the value of C_d is calculated for minimum V_{dc} (DC link Voltage) as

$$C_d = \frac{P_{min}}{2\omega\delta {V_{dc\,min}}^2}$$

$$= \frac{70}{2 \times 314 \times 0.04 \times 40^2} = 1741.6\ \mu F$$

The capacitor value should take higher than above value because the ripple voltages should be less than 4% even for minimum value of V_{dc}. So the selected value is 2000 μF for this application. In this application capacitor has to operate with high current and low frequency switching that why best suited capacitor is electrolytic.

E. Design of filter capacitor C_f and inductor L_f

Radzoun. [8] Calculated the value of C_f and L_f as

$$C_f < C_{max} = \frac{I_{peak}}{w_L V_{peak}} \tan(\emptyset)$$

Table 1 Simulated results for the suggested drive, varying speed.

$$= \frac{(\frac{350\sqrt{2}}{220})}{314 \times 220\sqrt{2}} \tan(1°) = 401.98\ nF$$

Where the I_{peak}, V_{peak} and $\emptyset$ are the peak supply current , peak voltage ,and the angle between the supply current and voltages respectively. The value that is selected for this application is 330 nF.

$$L_f = L_{req} + L_s \Rightarrow \frac{1}{4\pi^2 f_c^2 C_f} \qquad (11)$$

$$= L_{req} + 0.04\left(\frac{1}{\omega_L}\right)\left(\frac{V_s^2}{p_0}\right) \Rightarrow L_{req}$$

$$= \frac{1}{4\pi^2 f_c^2 C_f} - 0.04\left(\frac{1}{\omega_L}\right)\left(\frac{V_s^2}{p_0}\right) = 1.57mH$$

Where fc is the cut off frequency selected as

$$f_{sw} < f_c < f_L$$

Therefore, the value of f_c, is taken as $f_{sw}/10$ to achieve electronic commutation at fundamental frequency for switching of voltage source invertor.

V. Suggested BLDC drive simulated results

The results for the suggested drive are simulated in MATLAB-Simulink environment for improved performance over a wide speed range. Some factors related to BLDC drive and zeta convertor i.e. Switches current and voltage (v_{sw} and i_{sw}), centered capacitor voltage (V_{c1}), inductor currents (i_{L1} and i_{Lo}), stator current (i_a), electromagnetic torque (T_e), speed (ω), DC link voltage (V_{dc}), supply current (i_s) and supply

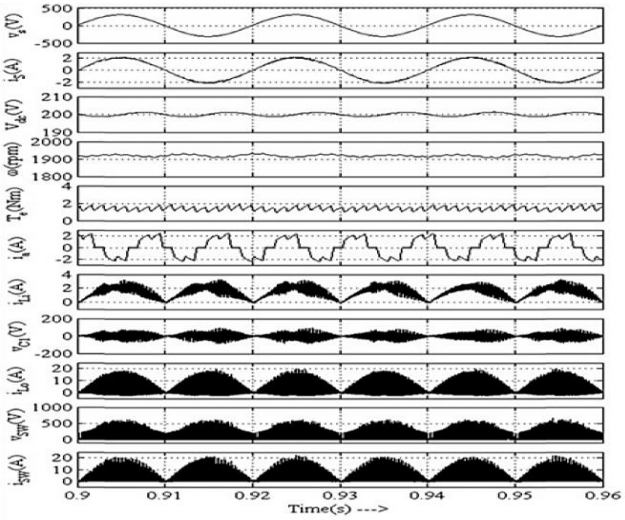

Fig 6 Steady state results of BLDC drive when Vs 220V and V_{dc} 200V

voltages (V_s) are explained the performance of model. Further to explain the enhanced power quality of the drive

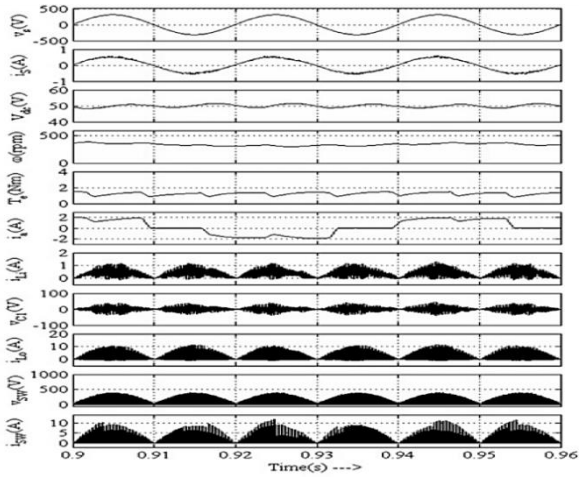

Fig 7 Steady state results of BLDC drive at Vs 220V and V_{dc} 50V

PF (power factor) and THD of i_s are also observed. Suggested drive simulated results are as follow.

4146 ISSN 1013-5316;CODEN: SINTE 8 Sci.Int.(Lahore),28(4),4141-4147,2016

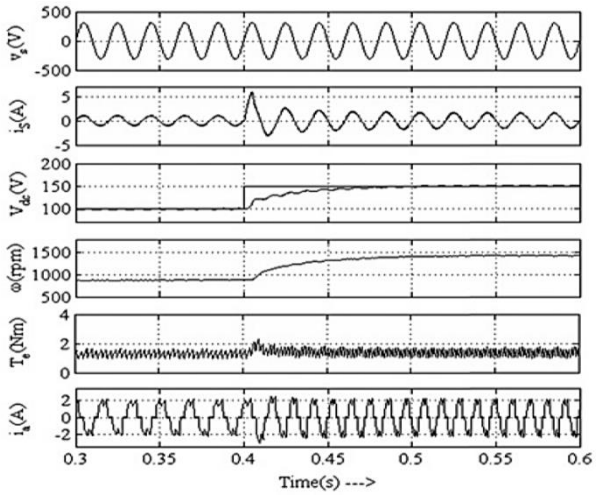

Fig 8 Changing V_{dc} from 100 to 150V

A. BLDC drive in steady state

The results obtained at steady state conditions at rated torque with V_{dc} 200V and 50V are in figs 6 and b respectively. The supply voltage and supply current obtain are in phase which demonstrate the PF is unity at AC main. A discontinuous current in inductor i_{Lo} and a continues current in i_{Lo} are obtained which shows the DCIM operation of Zeta. And the obtain THD of i_s is within the limits of IEC 61000-3-2 [3]. The results of the suggested drive are tabulated in Table 1.

Table 1 Simulated results of suggested drive, varying speed

$V_{dc,}$ V	RPM	THD% of i	PF	Is, A
50	350	5.6	0.84	0.29
80	700	3.6	0.85	0.56
110	910	2.8	0.87	0.83
140	1330	2.6	0.91	1.02
170	1710	2.45	0.93	1.31
200	1950	2.3	0.93	1.46

Table 2 Simulated results at different supply voltages

Vs, V	THD% of i_s	PF	Is, A
170	2.1	0.82	1.94
190	2.13	0.83	1.72
210	2.63	0.86	1.56
230	2.69	0.90	1.45
250	2.75	0.91	1.39
270	2.92	0.94	1.22

B. Results at different supply voltages

For the complete range of supply the improved power quality is displayed in table 2.

C. Dynamic result of suggested drive

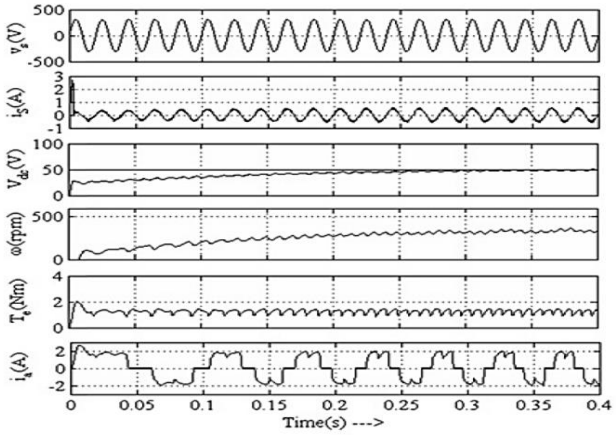

Fig 9 Dynamic result of BLDC drive at V_{dc} 50V

The dynamic result of drive at initial conditions and speed control is displayed in the fig 8 and 9, respectively. The performance when the starting of BLDC drive at 50V is displayed in fig 8. Further the performance of drive during step change in V_{dc} are displayed in fig 9. The control of V_{dc} limited transient stator and supply current during speed control and starting.

CONCLUSION

For the low power applications, the power factor improved zeta converter in front of BLDC drive is very effective and cheap solution. The suggested BLDC drive has been schemed for the controlled speed of wide range with enhanced power feature at AC source. A voltage follower topology is used to control the drive speed by varying the DC voltages at the input of invertor. This technique enables the switching of voltage source invertor on fundamental frequency for attaining an electronic commutation to minimize the switching losses. An improved zeta converter scheme work in discontinuous current mode leads a voltage follower topology to control the DC output. The results of the BLDC drive has been assessed for different input voltages and controlled speed.

REFERENCES

[1] J. F. Gieras, "Design of permanent magnet brushless motors for high speed applications," *Electrical Machines and Systems (ICEMS),* pp. 1-16, (2014).

[2] P. Kshirsagar and R. Krishnan, "High-Efficiency Current Excitation Strategy for Variable-Speed Nonsinusoidal Back-EMF PMSM Machines," vol. **48**(6), Nov-Dec (2012).

[3] "Limits for Harmonic Current Emissions (Equipment input current <16A per phase)," *International Strandard IEC 61000-3-2,* (2000).

[4] S. Jagadeeswari, N. Hemalatha and J. Baskaran, "PFC Bridgeless buck-boost converter-fed BLDC motor drive," *Computation of Power, Energy Information and Commuincation (ICCPEIC),* pp. 171-176, (2015).

[5] S. M. Madani, Lei Hao and H. A. Toliyat, "A low-cost four-switch BLDC motor drive with active power factor correction," *(IECON) Industrial Electronics Society,* vol. **1**, pp. 579-584, (2002).

[6] V. Krishnaveni, K. Kiruthika and S. S. Kumar, "Design and implementation of low cost four switch inverter for BLDC motor drive with active power factor correction," *Green Computing Communication and Electrical Engineering (ICGCCEE)*, pp. 1-7, (2014).

[7] S. Singh and B. Singh, "A Voltage-Controlled PFC Cuk Converter-Based PMBLDCM Drive for Air-Conditioners," *IEEE Transactions on Industry Applications*, vol. **48**(2), pp. 832-838, March (2012).

[8] R. Radzuan, M. A. A. Raop , M. K. M. Salleh and M. K. Hamzah, "The designs of low power AC-DC converter for power electronics system applications," *Computer Applications and Industrial Electronics (ISCAIE)*, vol. **14** (7), pp. 113-117, (2012).

[9] Y. H. Zhang, Zhang and X. Ma, "Distortion Behavior Analysis of General Pulse-Width Modulated Zeta PFC Converter Operating in Continuous Conduction Mode," *IEEE Transactions on Power Electronics*, vol. **27**(10), pp. 4212-4223, (2012).

[10] B. Singh, S. Singh, A. Chandra and K. Al-Haddad, "Comprehensive Study of Single-Phase AC-DC Power Factor Corrected Converters With High-Frequency Isolation," *IEEE Transactions on Industrial Informatics*, vol. **7**(4), pp. 540-556, Nov (2011).