# COPPER FILLING OF PRINTED CIRCUIT BROAD (PCB) INDUSTRY: A REVIEW

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***ABSTRACT:*** *With the increasing trend of miniaturisation in the industry, the rising pressure from both the device size and performance forces manufacturers to decrease device size while simultaneously increasing performance. In order to fulfil the demand, the application of copper via filling is one of the methods to achieve the milestone. In this paper, the introduction of the copper filling was presented. The filling parameters such as pressure flow, agitation, current density and additive concentration that affect the quality of via filling were reviewed and highlighted. Besides that, the properties of via and characteristic of copper via filling were also discussed in this paper.*

**Index Terms:** Bottom-up filling, Copper via filling, Microvias Printed Circuit Broad (PCB).

## I. INTRODUCTION

Printed circuit boards (PCBs) are commonly used in aviation, automotive, and the manufacture of medical equipment, electrical appliances, and mobile electronic devices, among others [1]. It is the media for the final interconnections among all completed chips and serves as the communication link between the component and microelectronic circuitry within each packaged integrated circuit. The PCB also connects circuit components such as resistors and capacitors. To ensure proper connections, all components are usually soldered onto the PCB [2].

The advancement of PCB was attributed to Paul Eisler, which is commonly known as the father of PCB. At the year 1941, He had made a great innovation of PCB, which is the transferred of PCB production from laboratory scale to full-scale production [3]. However, the origin of PCB needs to trace back to 20 years before Paul Eisler's contribution. During 1925, Ducas [4] found an alternative way to manufacture electrical conductors without using the winding of individual strands of wire. This was the first concept that formed the early stage of PCB. Not long after that, Parolini [5] has developed a new layout of PCB which is making a printed circuit by using U-shaped pieces of metal act as bridges at intersections of tracks.

At year 1967, Samuel [6] had invented a new method to connect the conductive layer through a hole. To connect between different layer of copper, a hole is drill on a PCB and a layer of copper is deposit on the hole wall. This invention able the current connects between layers while the drilled hole act as a path way for the current to pass through. Therefore, the drilled hole is also wildly call as 'via' which means road or pathway in the Latin word [7].

All of this invention had greatly increased the capability of circuit broad and lead to the creation of first prototype of modern PCB. The innovation will eventually affect the development of modern PCB in the future [3].

Fast forward to the modern world, product miniaturization has become a rising trend around the industry [8]. Especially with the rising of through hole electrical interconnections and SMT (surface mount technology) at 1980s [9], the pace of product miniaturise had been accelerated faster than ever. Along with the prediction of Moore's Law [10], the market also expects that newly released devices will double their performance every 2 years. The rising pressure from both the device size and performance forces manufacturers to decrease device size while simultaneously increasing performance. However, with the limitation of 2D packaging technology, the dimension miniaturisation and the performance enhancement of the component had reach to a bottleneck [11]. This phenomenon has forced PCB manufacturers to convert their manufacturing methods from 2D into 3D packaging [12]. As time passes, the production methods used for PCB are no longer the same as 50 years ago.

At present, PCB are usually made in multilayers, with an electrical conductive material layer acting as a conductor and a few layers of insulator materials in between acting as dielectric [13]. These insulator is usually made by glass fiber reinforce polymer, epoxy, polyimide and carbon fibre reinforced polymer [14]. Meanwhile, In order to ensure the best conductivity and low production cost of PCB, the electrical conductive layer is usually made by copper[15]. This is due to copper is a very common material in earth and it is also excellent in electrical conduction properties [16] .

In order to deposit a layer of copper in the wall hole, the via of PCB will go through plating process so that a thin layer of copper will plated on the wall of the hole. It is one of a very important process that able to deposit certain material on a subtracts [17]. Due to plating process is mostly happen in molecular level, it means the plating will able to reach within the narrowest place, this process properties is very useful in manufacturing miniaturised products, especially in the PCB industry [18].

However, the plated thin copper layer tends to crack or deform when stress or bending is applied on the PCB. Cracks severely affect the PCB performance, such as causing signal loss on the data transfer and voltage drop through the circuit. This problem can even shorten the PCB lifespan. Therefore, to avoid the problem created by plating, copper filling has been applied to the industry to resolve the limitations of the current PCB [19].

## II. PROPERTIES OF VIA

### A. Types of Via

The PCB industry manufactures two types of via, through hole and blind via [20]. Through hole is a via that penetrates from the top until the bottom of the PCB, whereas the blind via only drill until half way through the PCB. Fig. 1 shows images of the through hole and blind via.

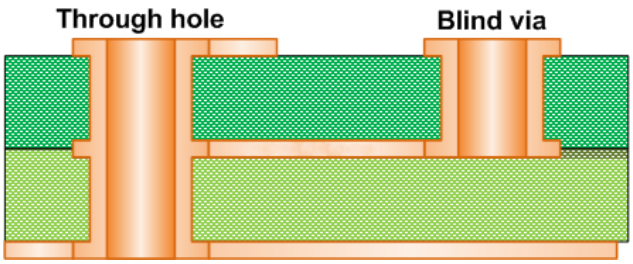



**Fig. 1:** The diagram of through hole and blind via [21].

### B. Diameter of Via

During the copper filling process, a larger via diameter causes formations of bigger dimples [22]. From the study of Feng et al. [23], the results indicated that increasing the via diameter also required a longer time to fill the via, thereby resulting in a thicker copper layer on the panel surface.

Similar with the discovered of Ma et al. [24], they stated that the diffusion time in electroplating process became shorter with larger via diameter. Whilst the diameter and the depth is 2.5µm and 50µm, the diffusion time in electroplating process is 15mins. However, if the via diameter and depth is only 25µm x 300µm, the diffusion time in electroplating process is only 2 mins for the process. Fig. 2 shows the result of Ma et al. [24].

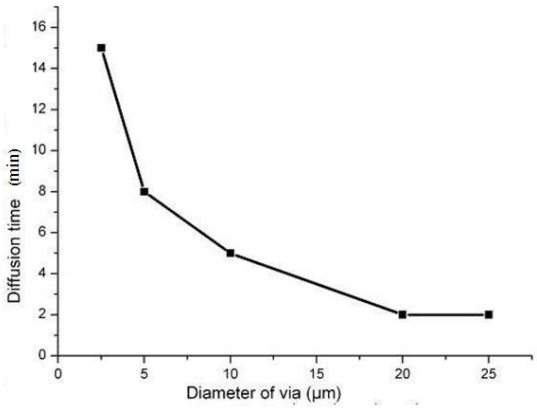



**Fig. 2: Diffusion time on bottom up filling [24].**

## III. COPPER FILLING

Copper filling is a new method for 3D-stacked packaging technology and is thus widely investigated. Copper is deposited in a bottom-up or superfilling mode to ensure the voidless filling of the via [25]. This process provides numerous advantages such as the avoidance of short circuits, reduction of current leakage, and prevention of electromigration [26].

Until now, copper filling is the most promising 3D packaging technology because of its advantages of small form factor, light weight, high density, low power consumption, and good electrical performance by interconnecting chips along the shortest vertical path [27].

### A. Electroplated Copper Filling

Electroplated copper filling is a type of galvanic plating method that relies on an external electrical power source to provide an ionic metal gaining electron. The charged ionic metal will then deposited onto cathode in order to form a coating on the workpiece [28]. This type of filling will usually involves a chemical solution that contains iodised form of metal in it. A positive charge is supplied to an anode and a negative charge from a cathode. This provided a current that trigger the chemical reaction of the metal ion and deposited a firm coating on the workpiece surface. The desired levels of thickness can be attained by controlling the processing time [28].

There are few researchers have innovated the via-filling process by using a different approach on the process setting, where Ishikawa et al. [29] have invented a simplify process procedure method while Jung et al. [30] have applied pulse reverse current mode instead of the conventional direct current mode. Zhu et al. [31] also developed a numerical model which was able to simulate the behaviour of copper electrodeposition process.

### B. Electroless Copper Filling

Unlike the electroplating method, electroless plating is a non-galvanic or auto-catalytic plating method to fill up the via of the PCB [32]. This method does not rely on external power sources, but instead depends on the natural attraction between oppositely charged ions. The ion is then deposited onto the subtract surface by the reduction or oxidation of the charges. Therefore, with the whole process independent of electricity, one of the main differences of electroless plating from electroplating is that it works on both conductive and nonconductive surface[28].

However, this process presents several drawbacks. The thickness produced by electroless plating is very thin compared with to electroplating method. It is also very sensitive to temperature and pH levels, which can potentially increase the running cost of the process.

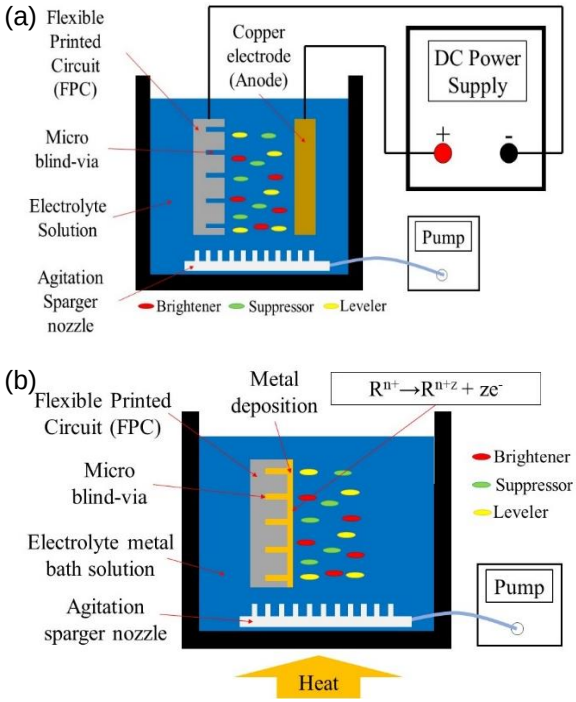
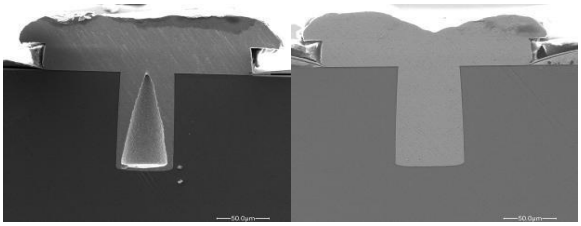



**Fig. 3: The schematic diagram of (a) electroplating and (b) electroless via filling respectively [32].**

In the study of electroless copper filling, Abe et al. [33] proved that via-filling can be achieved by electroless copper plating while Wang et al. [34] investigated that the effect of additives on hole filling by electroless plating. Fig. 3 shows the schematic of electroplating and electroless via filling methods.



(a) (b)

**Fig. 4: Via filling under different current density: (a) 0.5ASD, (b) 0.1ASD [40].**

## IV. FILLING PARAMETER

### A. Pressure and Solution Flow

Pressure and flow represent the force flow of the chemical bath during the filling process. This can prevent the mass transport from being limited by the increased solution exchange of the bath. To achieve a quality PCB, the flow of the solution bath has been proven as one of the essential parts of the process [35].

In the study of Engelmaier and Kessler [35], an experiment of force flow agitation on copper electroplating has been investigated. During the experiment, an 80-liter forced flow plating system wasbuilt to carry out the plating process. A pump was installed to force the solution exchange constantly and the flow was controlled in between 0 cm/s to 87 cm/s. At the end, the result shows that the present of agitation flow has created a much lower plating
resistance compared to the process without agitation flow. However, they also stated that, although the present of agitation could help to improve the process, but increase the flow beyond the necessary level (17 cm/s) does not further improve the quality of the deposited.

### B. Ultrasonic and Air Agitation

Ultrasonic refers to the sound waves with frequencies higher than the upper audible limit of human hearing; a sound that reaches 20 kHz or above is considered as ultrasonic while air agitation is the pumping of air into the bath to achieve the solution exchange of the bath solution. In the PCB industry, ultrasonic sounds are widely used as an agitation tool to force the bath solution exchange [36]. Additionally, ultrasonic agitation will also causes cavitation phenomena such as acoustic streaming, micro jetting and shock waves, which will achieve the surface cleaning, and mass-transfer enhancement between the anode and cathode [37]. These phenomena significantly improve the PCB quality during the plating and filling process.

In the year 2017, Wang and his co-worker [38] conducted the research by using ultrasonic agitation (20 kHz) during the process, which they found that the process able to achieve a higher filling ratio at a higher current density while maintaining the high quality of the via filling. In a same vein, Wang et al. [11] also found that an increase of copper deposition rate is driven by the increase of the power of ultrasonic agitation.

### C. Current Density

Current density is the amount of current that passes through a certain area. In the PCB filling, this area is determined by the exposure area of PCB in the filling bath solution. An increase in deposition rate is driven by the increase of current density, which may result in the raising of filling rate of the PCB owing to the faster deposition of copper [39]. However, the increase in current density also increases the chance of voids and seams appearing in the filling. The higher deposition rate increases the thickness of the wall hole, which eventually cause the top part of the via to close before the bottom part is completely filled [36].

Zhu et al. [31] developed a numerical model which able to simulate different current density of copper electrodeposition process. Whereas Wang et al. [36] claimed that the higher the current density will have a tendency to create a void in the via fill. The result is similar with the study of Miao et al. [40] which showed that the via filling with current density of 0.1 ASD able to achieve a better filling compare with the via with 0.5 ASD which a cone shape void has occur during the filling. Fig. 4 shows the via filled by different current density.

### D. Brightener

A brightener or accelerator is an organic material [20] that mainly functions to enhance the current density on certain areas of PCB. This material also acts as a microleveler and impact grain refiner which may help produce a very smooth and fine plating surface [30]. In the industry, the chemicals normally uses as brightener are mercaptopropyl sulfonic acid (MPS) and bis (sodiumsulfopropyl) disulphide (SPS). During the filling process, the brightener is added into the filling bath to increase the deposition rate at the via bottom and achieve the desired function such as superfilling or bottom-up filling [41].

An investigation of the behaviour of brightener has been conducted by Wu and Lee [42]. The experiment was conducted by ejecting 0.1 ml of brightener into 40 ml base electrolyte potentiostaticly at a -0.6V with the electrode rotating at 600 rpm. In the end, the accelerator inherent the system with the 1.1s of current density ascend rapidly, which shown that the addition of brightener will raise up the current density of the via filling process.

### E. Suppressor

The suppressor inhibits the deposition rate of PCB plating by reducing the current density of the plating area, thereby preventing the plated surface from becoming too thick. Examples of suppressors that are currently available are sulfopropyl sulfonate (SPS), poloxamine, polyethylene glycol (PEG) and chlorine ion [30], [43]. Moreover, suppressors similarly inhibit the copper deposition onto the wall hole during the via filling process, to prevent the filling of wall hole from becoming too thick and eventually closing the top part before the bottom part of the via is completely filled [44].

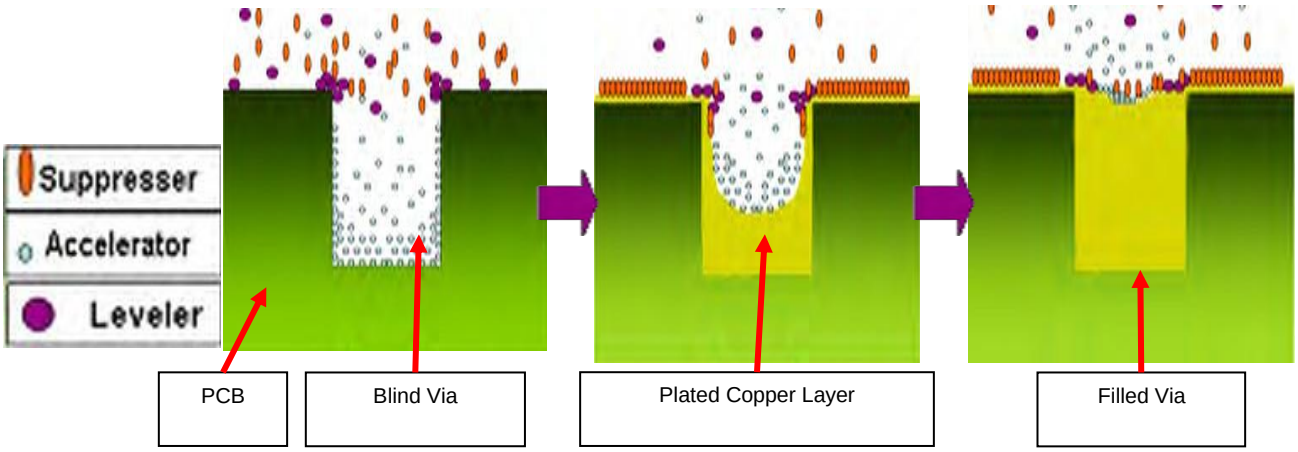



**Fig. 5:** Schematic sketch of via filling model ADDIN CSL_CITATION {"citationItems":[{"id":"ITEM-1","itemData":{"DOI":"10.1109/ICEPT.2009.5270791","ISBN":"978-1-4244-4658-2","abstract":"Copper electrodeposition in acidic cupric methanesulfonate bath with organic additives is discussed in this paper. The influence of poly(ethylene glycol) (PEG) and bis-(3-sodiumsulfopropyl disulfide) (SPS) on copper deposition were studied by means of linear sweep voltammetry, cyclic voltammetry and chronoamperometry. These electrochemical analysises revealed a competition of PEG and SPS on electrode surface site. The swiftness of SPS chemisorption and the subsequent displacement by the passivating film of PEG exerted an extra wave at small overpotential on the negative-going sweep. The following polarization curve indicated the firmness of the passivating film. All these features of additives in acidic cupric methanesulfonate bath suggested a novel method to achieve superconformal or bottom-up filling which was proved by actual TSV plating.","author":[{"dropping-particle":"","family":"Li","given":"Qi","non-dropping-particle":"","parse-names":false,"suffix":""},{"dropping-particle":"","family":"Ling","given":"Huiqin","non-dropping-particle":"","parse-names":false,"suffix":""},{"dropping-particle":"","family":"Cao","given":"Haiyong","non-dropping-particle":"","parse-names":false,"suffix":""},{"dropping-particle":"","family":"Bian","given":"Zuyang","non-dropping-particle":"","parse-names":false,"suffix":""},{"dropping-particle":"","family":"Li","given":"Ming","non-dropping-particle":"","parse-names":false,"suffix":""},{"dropping-particle":"","family":"Mao","given":"Dali","non-dropping-particle":"","parse-names":false,"suffix":""}],"container-title":"2009 International Conference on Electronic Packaging Technology & High Density Packaging","id":"ITEM-1","issued":{"date-parts":[["2009","8"]]},"page":"68-72","publisher":"IEEE","title":"Through silicon via filling by copper electroplating in acidic cupric methanesulfonate bath","type":"paper-conference"},"uris":["http://www.mendeley.com/documents/?uuid=a3d84d76-b5c4-4ca0-820b-a7f1b19c94c5"]}],"mendeley":{"formattedCitation":"[49]","plainTextFormattedCitation":"[49]","previouslyFormattedCitation":"[50]"},"properties":{"noteIndex":0},"schema":"https://github.com/citation-style-language/schema/raw/master/csl-citation.json"}[49]

Interestingly, there is some contradiction towards the function of sulfopropyl sulfonate (SPS). Shingubara et al. [44] claimed that SPS is act as a suppressor while some of them claimed that SPS is an accelerator [17, 31]. In the study of Lee *et al.* [45], they found that SPS has an accelerating and suppressing effect according to its concentration in copper electroless deposition. During the experiment, the SPS shows a highest acceleration (4.24 mA/cm) effect when the concentration is at 0.5 mg/l. But they also found out when the concentration of SPS increase to 5.0mg/l, the current density of the process will decrease (0.485 mA/cm).

Meanwhile, Wu and Lee [46] tried to achieve the copper filling by only using a single component suppressor system which has simplify the additive replenishment procedure of the process. Besides that, Wu and Lee [42] also investigated the behaviour of suppressor by injecting 0.4 ml of suppressor into 40ml of base electrolyte. The experiment was conducted potentiostaticly at a -0.6V with the electrode rotating at 600 rpm. The result shows that the suppressor taken 9.1s to plummet the current density greatly.

**F. Leveller**

Similar with brightener and suppressor, the leveller is also an organic additive. Most of the time, the leveller's function is to act as an inhibit reagents that suppress the copper deposition rate onto the PCB surface [47], to create a smoother surface and also reduce the chance of overdeposition above the superfilling or bottom-up filling region [48]. The difference between the suppressor and leveller is that the suppressor prevents the plating of PCB surface and wall hole from becoming thicker whereas the leveller prevents the copper deposition of the via filling from overflowing on the PCB surface and also prevent the top part of the via closing before the filling done.

In the study of Li et al. [49] clearly show the filling model and point out the function of different additive during the via filling, fig. 5 shows the explanation of the different additive during the via filling.

**G. Chlorine**

In the PCB industry, chlorine usually appears in the form of hydrochloric acid (HCl) or sodium chloride (NaCl) [50]. Apart from acting as a mild accelerator [50] , chlorine also acts as the stabiliser of the $Cu^{1+}$ ion. This serves as an intermediate in the electrodeposition process during reduction from $Cu^{2+}$ to $Cu^{1+}$. Additionally, chlorine modifies the adsorption properties of the carrier to influence thickness distribution [51].

Dow et al. [50] claimed that the reduction of $Cu^{2+}$ to $Cu^{1+}$ is a slow process while $Cu^{1+}$ is not stable and will easily return to $Cu^{2+}$ during the process. However, the $Cl^{+}$ will trigger the speed up of the $Cu^{2+}$ reduction by using its negative charge while also prevent the $Cu^{1+}$ revert back to $Cu^{2+}$. This result are likely related to the study of Bonou et al. [52] which they claimed that the adsorption of $Cl^{-}$ on the anode will cause the acceleration of $Cu^{2+}$ reduction.

## V. CHARACTERISTIC OF COPPER VIA FILLING

### A. Void

During via filling process, the top part of the via has better mass-transfer conditions and a higher current density than the bottom portion, which leads to faster deposition near the top. This causes the top part of the via to close before the bottom part is completely filled. Under this condition, the void defects will be formed in the via that can decrease device reliability and electrical performance after packaging [53].

Pan et al. [54] and Li et al. [55] investigated the effect of different pretreatments on through silicon via copper filling. Both of their result also showed that the application of ultrasound vibration and vacuuming method will greatly improve the via quality and avoid the happening of void.

### B. Dimple

A dimple is a small surface depression that occurs after the filling process, usually caused by underplating on the filled hole. The dimple may form due to contribute too much of leveller and suppressor in the plating bath, this will results in the filling unable to reach the surface [51]. Besides that, a via with bigger diameter will also have a bigger tendency to form a dimple on the via [22].

In the study of Roelfs et al. [56], the formation of dimple are largely affected by the current density and the diameter of the via. They claimed that a bigger diameter and higher current density will likely to form a bigger and deeper dimple during the via filling process.

### C. Bumps

Bumps are the occurrence of overfilling on the via and causing the top of the via to be higher than the PCB surface. This may cause difficulties for the PCB to stack on the filled micro via and eventually lead to the issue of planarisation in between [51], Moreover, the lack of leveller in the bath composition may also result in bumps occurring on top of the filling.

### D. Seam

The seam is a very small gap located right in the centre of the filled via. This occurs when the deposition rate of the hole wall is faster than the bottom part of the via. The seam may result in a void in between the PCB, which may also deteriorate the PCB quality in terms of lifespan, performance, and reliability. The application of ultrasonic agitation may increase the mass transport, thereby reducing the chances of forming a seam [36].

A study of different current density of 0.002 A/cm$^2$, 0.005 A/cm$^2$ and 0.008 A/cm$^2$ have been conducted by Wang et al. [36]. They found that only the 0.005 A/cm$^2$ has the highest chance to occur a seam during filling. This may be due to when the current density is 0.005 A/cm$^2$, the filling process will enter a conformal filling mode, which is also the cause that make the seam happen during the filling process.

## VI. CONCLUSION

The purpose of this paper is to review the previous research on copper via filling process. The introduction and type of via filling process have been briefly described and discussed in this paper. Based on the literature review, the significant filling parameter that effect of the behaviour of via filling have been reviewed and highlighted. The properties and characteristic of the process have also been reviewed and discussed.

The following conclusion show the significant outcome from the previous study:

- Current density, solution agitation and pressure flow are the most significant parameter to control the quality of the copper filled via.
- The concentration of the chemical additive (brightener, suppressor and leveller) has a significant result toward the coating surface.
- By controlling on the process, a defectless copper filled via will be produce by applying the optimised process parameter.

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