# IMPACT OF DIELECTRIC MATERIALS ON FinFET CHARACTERISTICS AT 45nm USING SILVACO ATLAS 2-D SIMULATIONS

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***ABSTRACT:*** *In this paper, the characteristics of different dielectric materials applied to 45nm Double Gate Fin Field Effect Transistor (DG FinFET) are studied by using the Silvaco Atlas 2-D simulations. An increase in the dielectric constant, it reduces the leakage current and improve the Short Channels Effects (SCEs) like Drain Induced Barrier Lowering (DIBL) and improve the Subthreshold Swing (SS). Gate dielectric materials such as $SiO_2$, $Si_3N_4$, Sapphire, $Ta_2O_5$ and $TiO_2$ are used to analyze various electrical characteristics at 45nm DG FinFET. The analysis included the threshold voltage, SS, DIBL, leakage current, surface scattering and mobility at 45nm DG FinFET with different gate dielectric materials.*

**Keywords**: dielectric, double gate, subthreshold swing, short channel effects, drain induced barrier lowering.

## 1. INTRODUCTION

For the past decades the advancements in the electronics industry have been primarily based on down-scaling the minimum transistor size according to Moore's law. However, scaling of conventional Metal Oxide field Effect Transistor (MOSFET) devices is limited due to SCEs, gate insulator tunneling and limited control of doping concentrations. MOSFETs are scaled primarily due to increased packing density and speed [1-2]. Due to scaling some negative effects predominate in conventional MOSFETs. They are mobility degradation and surface scattering, velocity saturation, avalanche breakdown, hot electron effect, DIBL, reduction of threshold voltage and punch through. These negative effects are known as SCEs. The SCEs with the conventional MOSFETs are increasing as devices becoming smaller. To overcome these difficulties, several alternative MOSFETs have been proposed by researchers such as DG FinFET, Trigate, and Foregate. DG FinFET integrated with a high-k gate dielectric is a promising device in the subthreshold region [3-4]. In this work the main focus is on investigating the electrical characteristics of DG FinFET such as threshold voltage, SS, DIBL, leakage current, surface scattering and mobility at the 45nm DG FinFET with reference to different dielectric materials.

The characteristic of the DG FinFET is that the conducting channel is wrapped around a thin silicon "fin", which forms the body of the device. The dimensions of the fin determine the effective channel length and gate width of the device. The thickness of the fin is measured in the direction from source to drain to establish the effective device channel length. The gate in a FinFET is wrapped around a thin silicon fin to exercise more control over the conducting channel. DG FinFETs are the most promising device structures to address SCEs and leakage issues in deeply scaled CMOS, as FinFETs can be fabricated using conventional CMOS processes and because these can be made in a self-aligned process [5-6]. Moreover, the FinFET is an ultrathin body device which eliminates the need of channel doping, thereby reducing parametric spread due to dopant fluctuations and reducing junction leakage due to high electric fields.

## 2. LITERATURE REVIEW

DG FinFET is one of the capable device to lengthen the technology of CMOS further to the limit of scaling of conventional CMOS technology. It is also an alternative device to overcome effects without deteriorating the device performance [7]. The semiconductor industry has been striving to present high-k gate dielectrics in the manufacturing double gate transistor process, so as to have less leakage current while caring for power consumption under control. Gate dielectrics are used in DG FinFET to prevent the current flow through the gate. Higher gate dielectric materials will have low leakage current, higher drain current, and also enhances the electrical characteristics of the devices [8-9]. In addition, higher gate dielectric is more preferred for nanoscale devices.

DG FinFET n-channel structure electrical characteristics and their reactivity dielectric materials of the gate with Gallium Arsenide as a substances of the channel were investigated [10]. At low supply voltage, the material of the channel can enhance the performances and speed of DG FinFET due to their device on-currents and higher electron mobility. By reducing the dimensions of devices in order to lead Moore's law International Roadmap for Semiconductors (ITRS), enhancement of performance and speed of FinFET at low supply of power is possible by utilizing material of the new channel other than Silicon [11]. Performance of various types of high-k dielectrics as the oxide of the gate for a 12nm Gallium Arsenide based DG FinFET was investigated [12].

A study of DG FinFET was done at 60nm with various type of high-k dielectrics compared with conventional MOSFET in terms of leakage current reduction. The FinFET with 60nm is created for high and low-k dielectrics. In this case, $SiO_2$ and $Hfo_2$ are utilized as high-k and low-k materials correspondingly [13]. New device materials are required to increase the CMOS technology usage further to 14nm node technology that can improve the performance of DG-FinFET. Various high-k dielectric materials are explored as the gate oxides in a 12nm SOI FinFET and the performance potential of gate dielectrics for Si based DG FinFET [14].

Nanoscale n-channel double gate FinFET structure electrical characteristics and their affectability to gate dielectrics material using Silicon, Germanium and Polymorphs of Silicon Carbide in the region of the channel. Investigation of nanoscale DG FinFET with material of the channel either of Silicon, Germanium and Polymorphs of Silicon Carbide. The influence of gate dielectrics on electrical characteristics were explored [15]. High-k dielectrics exhibits the best material and can restore other dielectrics material as it provides high transconductance ($g_m$), increase threshold voltage ($V_{th}$), reduce DIBL and SS. The utilization of high gate dielectrics enables the devices scaling.

## 3. DEVICE STRUCTURE

Various parameters of the proposed DG FinFET structure implementation used in this work are:

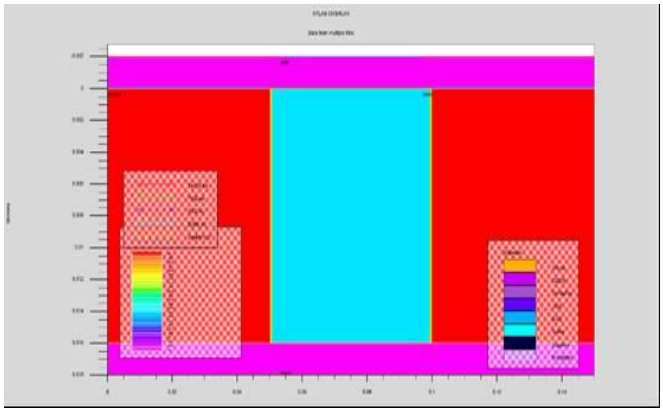

**Fig. 1. 2-D Double Gate FinFET structure**

$L_g$ is the length of the channel or gate between source and drain electrodes. $W_{th}$ is the width of the channel. $L_s$ and $L_d$ is the source and drain extension length. It decides the significant and capacitance of source or drain device resistance. $T_{ox1}$ and $T_{ox2}$ are material of oxide of gate thickness situated on either side of the channel through which contact of gate is made. The DG FinFET structure can be characterized in terms of fin length ($L_g$) and fin thickness ($W_{th}$). The silicon material with P-type doping concentration of 1e+15 /cm$^3$, whereas source doping concentration and drain doping concentration is 1e+20/cm$^3$ and thickness of oxide is 2 nm. Silvaco TCAD simulator is used to carry out device simulation and process simulation.

The corresponding k values for several gate dielectric materials are displayed in Table I and parameters used for the present work of simulation are shown in Table II.

**Table I: Various dielectric materials with their associated dielectric constants**

| Dielectric Materials | Dielectric constant |
|---|---|
| $SiO_2$ | 3.9 |
| $Si_3N_4$ | 7.55 |
| Sapphire | 11.5 |
| $Ta_2O_5$ | 25 |
| $TiO_2$ | 85 |

**Table II: Different parameters of device structure**

| Device Parameters | Values |
|---|---|
| Length of the gate ($L_g$) | 45nm |
| Equivalent Oxide Thickness (EOT) $T_{ox1}$, $T_{ox2}$ | 2nm |
| Fin Width ($W_{th}$) | 16nm |
| Extension length to source and drain ($L_s$ and $L_d$) | 2.5 nm |
| Channel doping | 1e+15 /cm$^3$ |
| Drain/source doping | 1e+20 /cm$^3$ |
| Channel doping type | P |

## 4. RESULTS AND DISCUSSION

### 4.1 Threshold Voltage ($V_{th}$)

Charge sharing is the main source for $V_{th}$ roll-off. The $V_{th}$ variations for several high gate dielectric materials are shown in Figure 2. The higher value of $V_{th}$ is acquired for $TiO_2$ resulting in improved $V_{th}$ among these materials. The gate needs to carry less charge in region and the $V_{th}$ falls down thereby degrading performance of device. The threshold voltage begins to reduce as the length of the channel is shortening in CMOS devices because depletion region charge is supported by source and drain. From the graph, it is observed that the threshold voltage values for $SiO_2$, $Si_3N_4$, Sapphire, $Ta_2O_5$, and $TiO_2$ are 0.42 V, 0.44 V, 0.45 V, 0.47 V, and 0.49 V. As the gate dielectric materials increases, the threshold voltage increases too when $V_d$ = 0.1V.

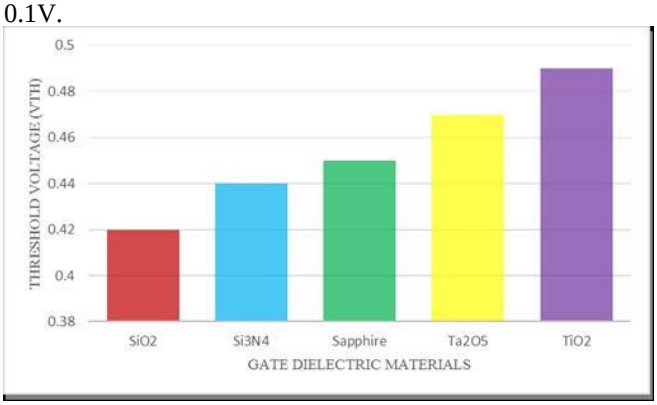


**Fig. 2. Threshold Voltage variation for different gate dielectric materials ($V_d$ = 0.1V)**

### 4.2 Sub-threshold Swing (SS)

The SS values for $SiO_2$, $Si_3N_4$, Sapphire, $Ta_2O_5$, and $TiO_2$ are found to be 67.6 mV/decade, 63.7 mV/decade, 62.3 mV/decade, 61.3 mV/decade and 60.8 mV/decade. It can be clearly seen that the sub-threshold swing for $TiO_2$ exhibits lowest value as a material of dielectrics with 60.8 mV/decade for DG FinFET, which has length of gate of 45nm. Reduced SS for $TiO_2$ due to its high dielectric and decrease in leakage current as shown in Fig. 3. Besides that, high gate dielectrics help to rise in the capacitance between gate and channel which result in enhances the sub-threshold swing and fewer leakage current between drain and gate. The capacitance rises by the gate dielectric constant, when a gate dielectric is included between semiconductor material and metal gate.

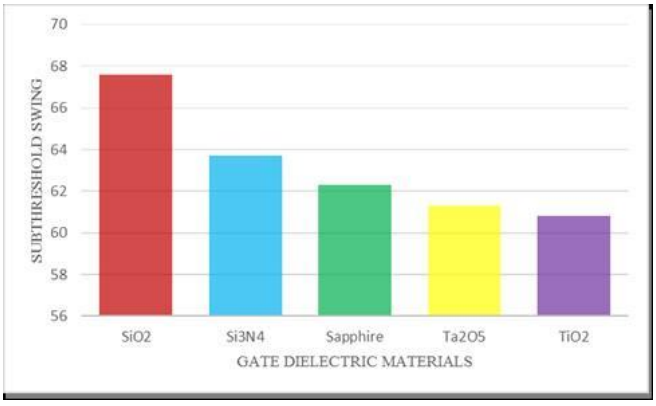


**Fig 3. Sub-threshold Swing variation for different gate dielectric materials. ($V_d$ = 0.1V)**

### 4.3 Drain Induced Barrier Lowering (DIBL)

DIBL in MOSFETs is referring originally to a reduction of threshold voltage of the transistor at higher drain voltages. The DIBL values for $SiO_2$, $Si_3N_4$, Sapphire, $Ta_2O_5$, and $TiO_2$ are found to 425mV/V, 411mV/V, 415mV/V, 413mV/V and 421mV/V. $TiO_2$ has shown 96% reduction in DIBL in comparison to $SiO_2$ as gate oxide material for DG-FinFET as shown in Fig. 4. The DIBL value for $TiO_2$ is quite appreciable and reveals that it exhibits better gate control over the channel relative to other dielectric materials. The reduction in the barrier junction of source, electrons are simply injected into channel and gate voltage has no longer any restrict over the drain current. Materials of oxide having high dielectrics are preferred for nanoscale devicessentence.

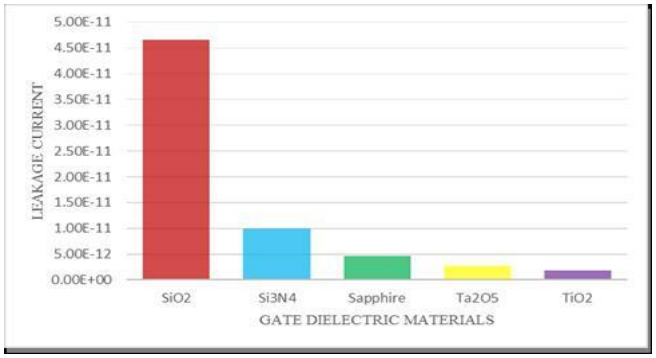


**Fig. 4. DIBL variation for different gate dielectric materials ($V_d$ = 0.1V and $V_d$ = 1V)**

### 4.4 Leakage Current

The DIBL values for $SiO_2$, $Si_3N_4$, Sapphire, $Ta_2O_5$, and $TiO_2$ are found to 4.6655e -11, 9.90569e -12, 4.75317e -12, 2.67717e -12 and 1.89816e -12. As $T_{ox}$ scales gate leakage current increases exponentially due to exponential increase of tunneling probability with reduction of physical tunneling distance. Physically thicker gate dielectric allows lower leakage current but lower oxide capacitance reducing on-current. Reduced in leakage current for $TiO_2$ is its high gate dielectric as shown in Fig. 5. Using high gate dielectrics material, both thicker physical thickness and higher oxide capacitance can be achieved. Applying high gate dielectrics, several orders of magnitude lower gate leakage current can be achieved with similar oxide capacitance.

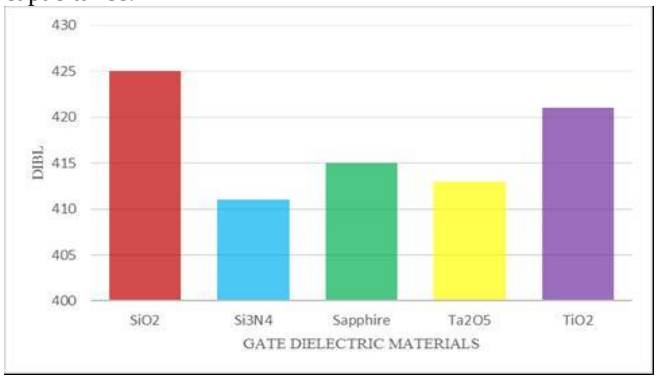


**Fig. 5. Leakage Current variation for different gate dielectric materials $V_d$ = 0.1V**

### 4.5 Mobility

Surface scattering of phonon in high gate dielectrics is the reason for mobile degradation. The mechanism of mobility degradation happen when high gate dielectrics has polarize metal oxygen bonds. When phonons and oscillations of gate plasma in high gate dielectrics are in resonance, oscillating dipoles interacts with carriers of channel. This condition of resonance helps to channel carrier mobility significant degradation. When density of gate carrier is 1e+19 /$cm^3$, resonance occurs. In order to avoid mobile degradation, use metal whose free density of carrier overreach 1e+20 /$cm^3$, condition of resonance is unsatisfied and reduces the interaction. Mobile degradation may increase from the soft optical phonons in the high gate dielectrics that react as "remote phonon scattering centers" and decrease mobility of channel. The mobility of channel in high gate dielectrics which is $TiO_2$ give arise to huge errors because of the carriers trapping as shown in Fig. 6.

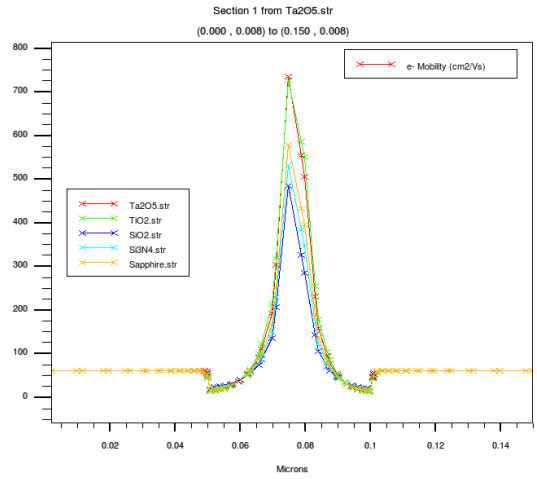


**Fig. 6. Mobility across channel length**

### 4.6 $I_d$ versus gate voltge ($v_{gs}$)

The gate dielectric $SiO_2$ is replaced with various high gate dielectrics. These gate dielectrics decreases the direct tunneling leakage current and give higher physical thickness. When the voltage of the gate increases, the drain current rises associated with increases gate dielectrics. $TiO_2$ has the high gate dielectrics as shown in Fig. 7.

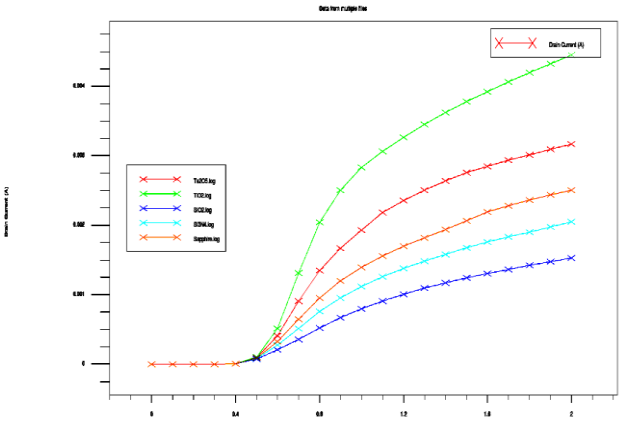

**Fig. 7. Drain Current ($I_{ds}$) Vs Gate Voltage ($V_{gs}$)**

### 4.7 Surface Scattering

The channel becomes smaller due to lateral extension of the depletion layer into the channel region as the mobility

of surface and longitudinal electric field component rises becomes field-dependent as shown in Fig. 8. The surface scattering causes degradation in mobility, the electrons move with great ease parallel to the interface. High dielectric material generates high electric field.

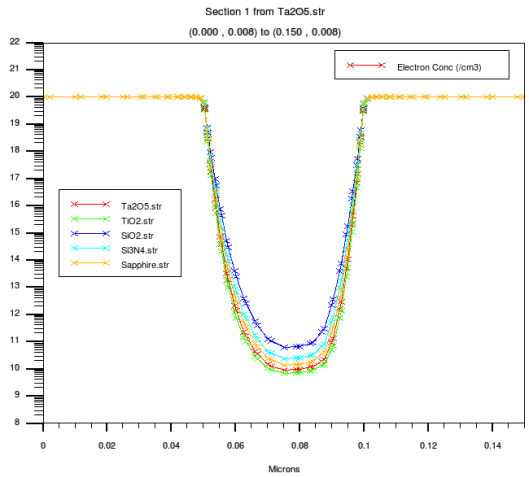


**Fig. 8. Surface Scattering across channel length**

## CONCLUSIONS

In this paper, the electrical characteristics of DG-FinFET structure have been studied and analyzed by applying various gate dielectric materials. $TiO_2$ as gate dielectric material shows enhancement in threshold voltage, and reduced short channel effects such as SS and DIBL. $TiO_2$ exhibits reduction of leakage current, SS, DIBL and mobility of channel and increase in the threshold voltage. $TiO_2$ improved device performance, better control of gate over the channel, reduction of the effective leakage current and offer high amplification values.

## REFERENCES

[1] International Technology Roadmap for Semiconductors. (2006)

[2] Cristoloveanu, S and Li, S.S., "Electrical Characterization of Silicon-on- Insulator Materials and Devices," Kluwer Publications, Boston, (1995)

[3] Celler, G.C and Cristoloveanu, S., "Frontiers of silicon-on-insulator," *Journal of Applied Physics*. 93, 4955 (2003).

[4] Colinge, J.P., Silicon-On-Insulator Technology: Materials to VLSI. Kluwer Publications, Boston, (1991)

[5] Haensch, W., Nowak, E.J., Dennard, R.H., Solomon, P.M., Bryant, A., Dokumaci, O.H., Kumar, A.,. Wang, X., J. B. Johnson, J.B., Fischetti, V., "Silicon CMOS devices beyond scaling," *IBM Journal of Research and Development*. 50, 361 (2006)

[6] Debajit Bhattacharya, Niraj K. Jha., "FinFETs: From Devices to Architectures," *Advances in Electronics*, Article ID 365689, (2014).

[7] Boukortt, N., Hadri, B., and Patanè, S., "Effects of High-k Dielectric Materials on Electrical Characteristics of DG n-FinFETs," *International Journal of Computer Applications*, 139: 28-32(2016).

[8] Das, R., Maity, S., Choudhury, A., Chakraborty, A., Bhunia, C., and Sahu, P., "Temperature-dependent short-channel parameters of FinFETs," *Journal of Computational Electronics*, 17: 1001-1012(2018).

[9] Patchrasardtra, N., and Pengchan, W., "The Influence of Gate Scaling to Electrical Characteristics on n-MOS FinFET," *MATEC Web Conf*. 108 09002 (2017).

[10] Bourahla, N., Hadri, B., and Bourahla, A., "3-D Simulation of Novel High Performance of Nano-Scale Dual Gate Fin-FET Inserting the High-K Dielectric $TiO_2$ at 5 Nm Technology," *Silicon*, 12:1301-1309(2019).

[11] Fatima Zohra Rahou, Guen Bouazza, A., Bouazza, B., "Effects of High-k Dielectrics with Metal Gate for Electrical Characteristics of SOI TRI-GATE FinFET Transistor," *Journal of Nano Electronics Physics*. 8(4/1): 04037(2016).

[12] Vinay Kumar, RPP Singh, Richa Gupta, and Rakesh Vaid, "Effect of High-k Gate Dielectric Materials on Electrical Characteristics of GaAs Channel Material Based Double Gate n-FinFET", *International Journal of Emerging Research in Management &Technology*. (2016).

[13] Flavia, I., Princess Nesamani and Rijo, P.C., "Performance Analysis of FinFET Device at 60nm", *International Journal of Engineering Trends and Technology*, 4(3): (2013).

[14] Vinay Kumar, Richa Gupta, Raminder Preet Pal Singh, and Rakesh Vaid, "Performance Analysis of Double Gate n-FinFET Using High-k Dielectric Materials", *International Journal of Innovative Research in Science,Engineering and Technology*, 5(7):(2016).

[15] Nour El Islam Boukortt, Baghdad Hadri, and Salvatore Patane, "Effects of Highk Dielectric Materials on Electrical Characteristics of DG n-FinFETs," *International Journal of Computer Applications*, 139(10): 2016.