PERFORMANCE EVALUATION OF EXTERNAL TERMINATIONS ON DUAL IN-LINE MEMORY MODULE DATA QUEUE OVER ON-DIE-TERMINATION

S. Assad, F.G. Awan, N. Inam
Dept. of Electrical Engineering, University of Engineering and Technology Lahore

ABSTRACT *This paper investigates and incorporates the use of external terminations on data signal of Dual In-line Memory Module (DIMM) and overall performance comparison in terms of reflection within the constraint put up by the space limitations on Printed Circuit Board (PCB). The key parameter, phenomenon of signal integrity (SI) has been properly ensured the first time working of the design. This further compares DDR2 DIMM implementation with and without the use of ODT. Several simulations of Data Queue (DQ) and Data Queue Strobe (DQS) signal, run in real- time environment are included for getting customized design*.

Keywords: On-Die-Termination (ODT), Data Queue (DQ), Field Programmable Gate Array (FPGA), Dual Data Rate (DDR2), Dual In-line Memory Module (DIMM), Eye Diagram

INTRODUCTION

In the modern application specific integrated circuits (ASIC), there is a flexibility to use the On-Die-Termination (ODT) to minimize the reflections without adding external terminations and by this way, the covered area on board with the supporting circuitry of that particular IC becomes small. This further cuts the cost of the overall system [1]. While implementing the DDR2 DIMM in a FPGA based System level Design, there are many signal integrity issues associated with the signal integrity and timing violations. While designing this interface, these issues must be considered in order to achieve desired results. A better signal integrity requires that the terminations should be correctly chosen for a particular cycle so that the receiver does not face any problem when the data is valid on receiver's input pin. Moreover, the data should be properly synchronized with the strobe signal to avoid meta-stability [2].

INVESTIGATION FLOW

This investigation gives us a comparison about DDR2 DIMM implementation with and without the use of ODT. There are certain limitations when we use the ODT and these limitations can be avoided by proper use of external termination. The paper includes several simulations of DQ and DQS signal that have been run in real-time environment at 533MHz. In these simulations, actual model of XILINX VIRTEX V FPGA and DDR2 micron DIMM have been used to extract the real scenario while interfacing a DDR DIMM and FPGA.

The models used in simulations represent the actual behavior of these ICs when implement in real environment and are taken from the chip manufacturers [2]. All the simulations are carried out at 533MHz with pre-layout topologies.

The design flow of the simulations involves the following steps.

a. DQ signal with external termination.
b. DQ signal with ODT.
c. DQS signal with external termination.
d. DQS signal with ODT.
e. Super-imposing the results of step 1 and step 3.
f. Super-imposing the results of step 2 and step 4.

TOPOLOGY AND SIMULATIONS

Simulations of DQ signal with external termination.

The topology of circuit when FPGA act as a driver and memory DIMM as receiver is shown in Figure 1. In this topology, there is an external tuned termination resistance to get a better working eye and signal swing for DQ signal. The working eye-diagram and output signal driving strength at the receiver are shown in figure 2 and figure 3 respectively.

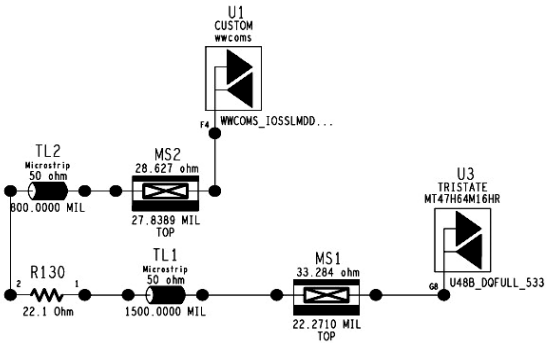

Fig 1. Circuit topology with external termination.

In this configuration, the IO model for DQ pin doesn't contain any on die termination. That's why there are external terminations used to get required signal quality and strength at receivers end. U1 is FPGA and F4 is its pin outputting DQ whereas U3 is the receiver DIMM and G8 is its IO pin.

Figure 2 shows the working eye diagram of DQ signal. The Vin (low) is 650mV and Vin (High) is 1.15 volts for DQ signal. Blue and aqua eyes indicate the eye at drivers end and eye at receiver's end respectively. Signal at driver's end is not considered significant from design point of view but there should be a clean signal with its working eye satisfying the proper voltage levels and there should be no glitch within that level [3]. The figure clearly shows that the working eye has sufficient window to fulfill the data level requirement for DDR DIMM.

The voltage swing at receiver's end is also very high indicating good drive strength. In figure 3, Blue indicates the signal strength at drivers end and Green indicates signal strength at receiver's end.

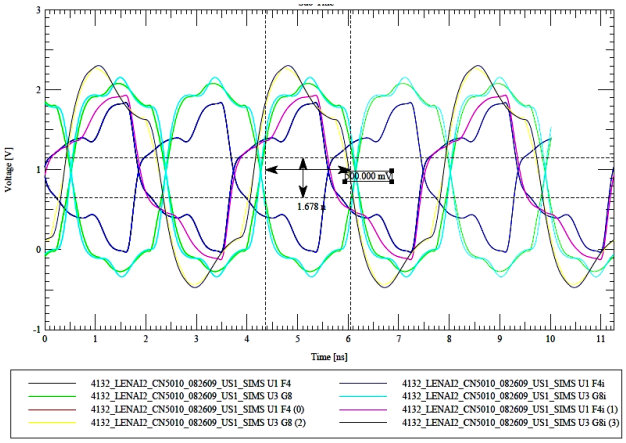

Fig 2. Working EYE of DQ driver and receiver. Voltage versus time

Fig 3. Output drive of DQ driver and receiver. Voltage versus time

The output drive at the receiver is 2.765 Volts, while the required DQ level at receiver is 1.150 volt high and 650mVolts low. This drive is sufficient to fulfill the signal requirement.

Simulations of DQ signal with ODT

Now consider the case when there is the use of ODT with no external termination while simulating DQ. The propagation delay which is a function of traces length is tolerable in this case as compared to a previous case in which there was an external resistor termination. This circuit topology is shown in figure 4. The memory model is different from the previous one. It contains the internal 50ohm ODT incorporated so there is no need for external termination.

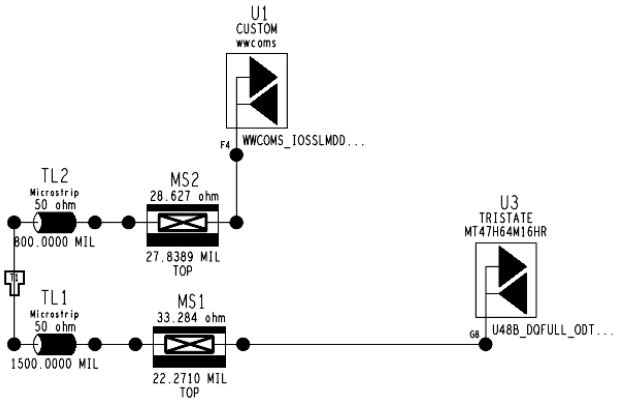

Fig 4. Circuit topology with 50 ohm ODT.

The output drive with this topology is shown in figure 5. The only comparative change is in the receiver model. The driver, frequency and the total data path length are the same. Here, blue indicates the signal strength at drivers end and aqua indicates signal strength at receiver's end.

It is evident from figure 5 that the output swing is much less than that of previous case. The maximum drive is 1.541 Volts at receivers end compared to output drive of 2.765 volts previously. The wave shape is comparatively better whereas the desirable functionality can also be achieved by using high voltage swing as in the previous case. Blue eye indicates the eye at drivers end and black eye indicates eye at receiver's end. Figure 6 shows the working eye on DQ with 50 ohm ODT.

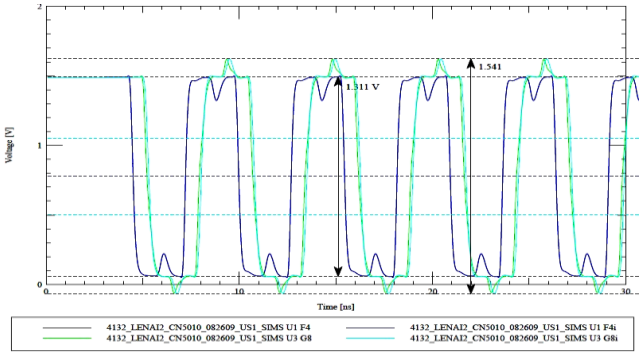

Fig 5. Output swing at receiver and drivers end.

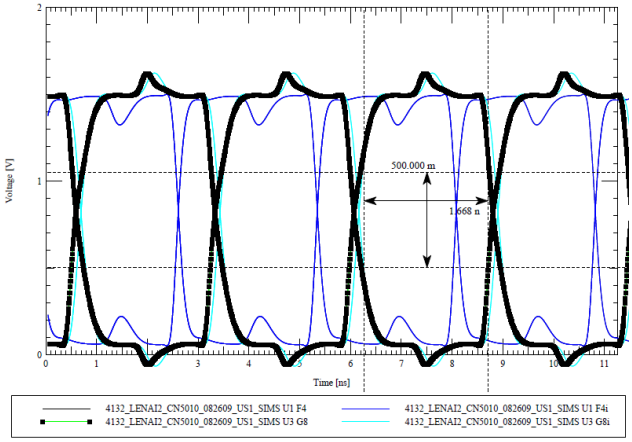

Fig 6. Showing the Eye diagram with 50 ohm ODT.

Simulations of DQS signal with external termination.

The next step is to simulate DQS with terminations so that there will be a clear picture about setup and hold time in both cases. Considering the DQS signal without ODT but with the external termination, the topology is shown in figure 7. In this case the length is also matched with DQ signal (with external termination). The output drive and working eye diagram is shown in figure 8 and figure 9 respectively.

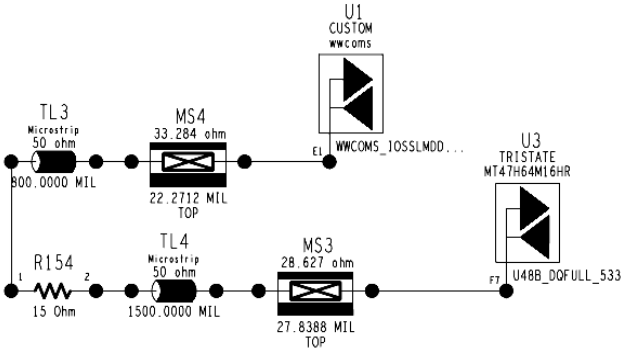

Fig 7. Topology of DQS with external termination.

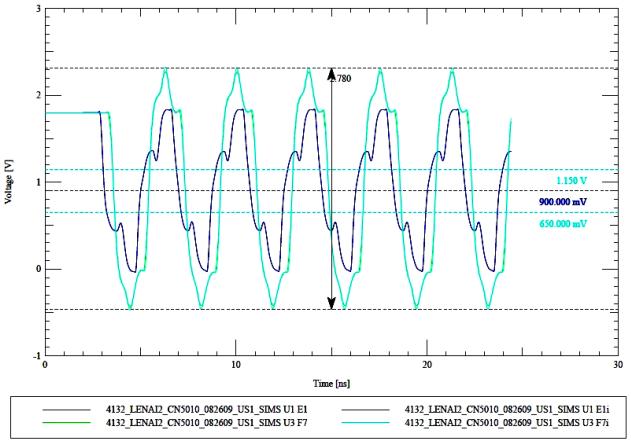

Fig 8. The output drive of DQS without ODT.

This case is similar to that of DQ without ODT. In figure 8, the nominal, low and high values of DQS signal are also given and the driving strength of DQS signal at receiver is also mentioned which is far more than the high value required for DQS signal. Blue represents driver's end and aqua representing receiver's end. This shows that there will be no signal attenuation if lengths of both DQ and DQS signal are matched and the DIMM is placed at some place far from FPGA. If any one of DQ or DQS signal has not achieved high driving power, then the DIMM may not route at a place far from FPGA due to the fact that one signal with less driving force will attenuate at the receiver and the signal with least driving force might not be fulfilling the minimum driving requirement at receiver.

Figure 9 shows the working eye region of the DQS signal without ODT with blue representing drivers end eyes and green representing receiver's end eye.

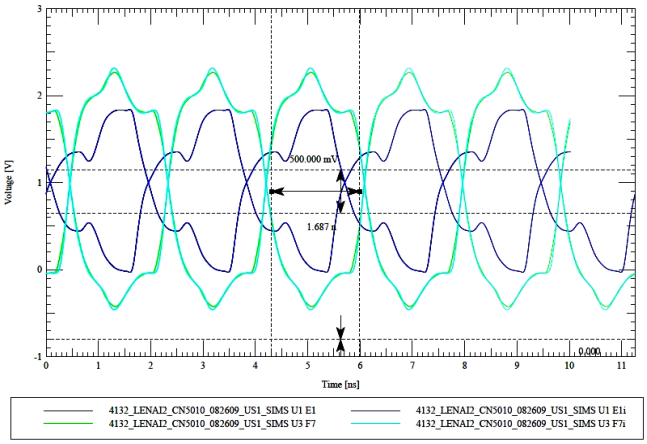

Fig 9. Working eye of DQS without ODT.

Simulations of DQS signal with ODT

Now consider the DQS signal with ODT, the circuit topology, driver's/receiver's signal strength and the working eye diagram are shown in figure 10, figure 11 and figure 12 respectively.

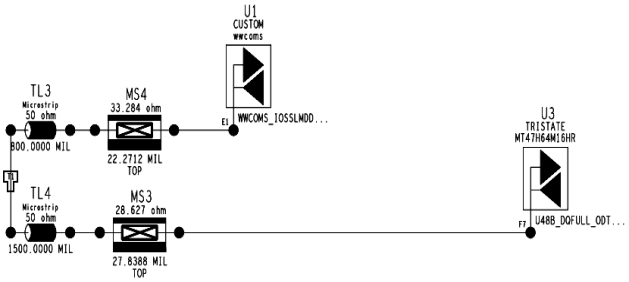

Fig 10. Topology with ODT.

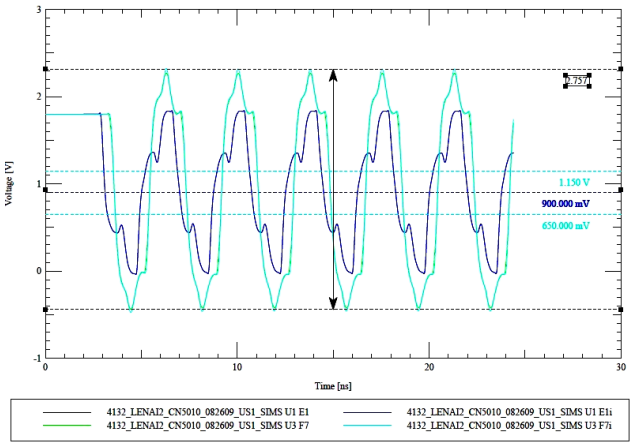

Fig 11. Driver's and receiver's ends signal swing. Blue represents the drivers end and aqua the receiver's end.

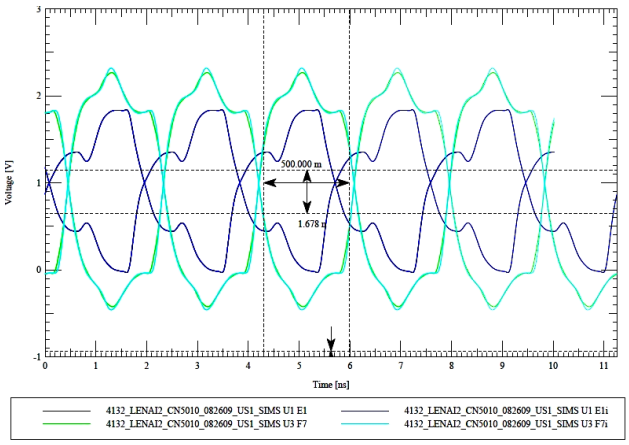

Fig 12. Eye diagram with ODT. Blue representing the drivers end and aqua represents the receivers end.

Super-Imposing the results of step 1 and step 3

To check functionality whether the two scenarios will work out same or differently, it is easier to see the setup and hold time for both cases. This is done by super imposing the DQS signal with DQ, with and without termination.

By superimposing the DQ signal with DQS signal at receiver's end with external termination included and by giving the DQS signal the offset of 0.7nsec, the results can be displayed in figure 13.

According to figure 13, the setup time is 734.154psec and the hold time is 924.640psec. Red and green representing the DQS and the DQ signals respectively.

Super-Imposing the results of step 2 and step 4.

Results of Figure 13 and figure 14 can be compared with that model output in which there is an ODT to validate the correctness of two models with same functionality.

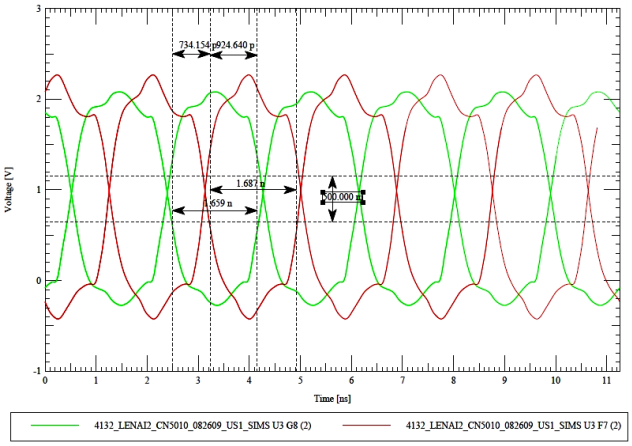

Fig 13. Setup and hold time without ODT.

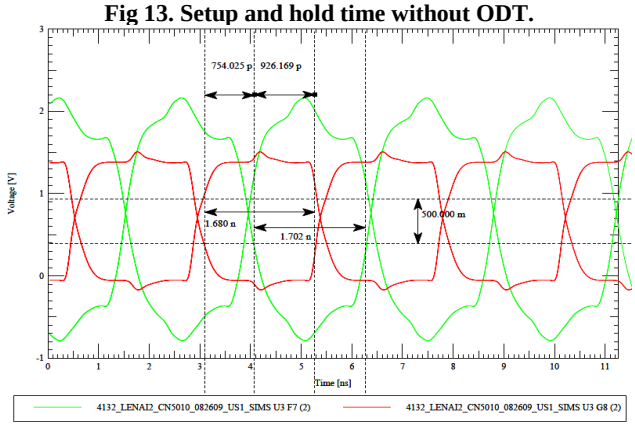

Fig 14. The setup and hold time with ODT. Green representing DQS and red represents DQ signal eye.

In figure 14, the setup time is 754.025 psec and hold time is 926.169 psec. These values are comparable to that of figure 13 with a small tolerable difference.

CONCLUSION

Design Flexibility with external termination.

No matter DQ at receiver with and without termination, have a much better eye, but by analyzing the waveform in both topologies, the output swing of DQ without termination is comparatively better than ODT case. The signal integrity with ODT is much better [4] but the driving power of DQ at the receiver with external termination is higher than required means that it is not necessary to place the DIMM near FPGA. This gives the flexibility in design that if we need to place the DIMM far from FPGA due to routing constraints on a very dense board, we can place our DIMM at some place far from FPGA. The signal will not attenuate due to very high driving power. If the designer has limited space on PCB to implement the DIMM, then the use of ODT is recommended, meaning thereby that the placement area is small and the designer doesn't have much space for the external termination and also there is no need for a very high signal drive at receiver.

Thus, while implementing it in PCB, we can have higher flexibility. Moreover, we can achieve the signal strength of our own choice by adjusting the routing length and value of termination resistance which is an additional benefit. It is also important that there should be no mismatch between the termination resistor for similar group of signal otherwise that may cause jitter [5].

Power Requirements.

Another benefit of using our external termination topology is that the input current requirement for our DIMM will be less as compared to that of DIMM in which we use ODT. This is due to fact that there is some biasing current required to our ODT. This may also cause overheating of DIMM.

The power consumption factor is only for a particular cycle and not when the IC is in standby or low power mode [1], and during read cycle only [2]. So, in-order to get rid of these issues in a flexible environment, we quantitatively justify the use of external termination.

Internally the Bias resistance is connected to Vtt. If we incorporate the ODT in our design, the additional current to bias the resistance can be calculated from the formula given below [3]

$$R_{TT}(EFF) = \frac{V_{IH}(AC) - V_{IL}(AC)}{I(V_{IH}(AC)) - I(V_{IL}(AC))}, (1)$$

It will increase with the number of ODT units that a memory has within its die. When we use the external terminations I-bias will be zero as there will be no Rtt (Internal termination resistance).

So we recommend using the ODT only when there is no other way but yet the better choice is to use the external termination to get more customized design.

ACKNOWLEDGMENT

The authors gracefully acknowledge the services and help of System Design laboratory UET Lahore for this investigation.

REFERENCES

[1] K. Kant, Data center evolution: A tutorial on state of the art, issues, and challenges, Hillsboro Oregon, USA, November 2009.

[2] ALTERA, *External Memory Interface Hand Book* vol **6**, Sanjose CA, November 2009.

[3] Micron Technology, Inc, MT47H64M16, *http://download.micron.com/pdf/datasheets/dram/ddr2/1GbDDR2.pdf*, 2009.

[4] HiTech Global,"*HiTech Global Virtex™-5 FXT/LXT/SXT Development Platform for PCI Express® Generation 1 & 2 Version 1.3",USA,* December 2008.

[5] S.Suresh and C.Panch**, "***How to become a hot commodity*", www.planetanalog.com, San Jose Bay, 2006.