STACKUP ARRANGEMENTSIN PRE-LAYOUT SIGNAL INTEGRITY ANALYSIS OF MULTI-LAYER PRINTED CIRCUIT BOARDS

Mamoona Tariqf[1]and Adil Farooq[2, 3]

[1]Department of Electrical Engineering, University of Engineering and Technology, Taxila, Pakistan
[2]Department of Electronic Engineering, International Islamic University, Islamabad, Pakistan
[3]The BioRobotics Institute, Scoula Superiore Sant'Anna, Pisa, Italy
∗For correspondence; E-mail: mamoona_tariq4@yahoo.com, adil.farooq@iiu.edu.pk

ABSTRACT: *This paper focuses on the elimination of signal integrity (SI) problems and the importance of the stackup arrangement by performing a pre-layout analysis. The pre-layout analysis includes consideration of I/O technology, chip packages, stackup arrangement, proper pin assignment and selection of clock topology. Two multilayer printed circuit boards, old and new versions, with different stackup arrangements are compared by analysing critical signals in Hyperlynx. In the old version, an inappropriate stackup arrangement causes reflection noise in some critical signals. The problem is then resolved by a correct stackup arrangement with impedance matching which removes reflection noise and ensures reliable transmission of critical signals.*

Key words: Signal Integrity Analysis, Stackup Arrangement, Reflection, PCB

1. INTRODUCTION

Most digital printed circuit boards are now multi-layered. The issues associated with signal integrity mostly occur in high-speed digital circuits [1].Impedance control for printed circuit boards (PCB) is one of the main concerns considering signal integrity. Other factors are the copper thickness of the circuit, conductor width, and the dielectric constant of the material. Circuit thickness is the main factor for impedance change during fabrication. In recent years more focus has been placed on insertion loss for digital PCBs. A higher insertion loss in a circuit will cause the signal to lose amplitude, significantly affecting the pulse shape. Therefore, the inclusion is worse for higher frequencies.

At low speeds, the frequency response has less effect on the signal [2]. However, the dissipation factor

Increases with an increase in frequency. Signal Integrity analyses of critical signals and corrective actions have been suggested [3]. Distributing control signals, power and ground through high-speed interconnect and complexity is challenging. Most of the research work has been aimed at reducing delay and power dissipation only [4]. Noise effects such as Crosstalk induces overshoot at a noise-site causing a coupling effect which can damage the chip permanently [5]. To reduce crosstalk, interconnects are kept in adjacent metal layers orthogonal to each other. Other general methods for reducing the effects of crosstalk include wire spacing adjustments [6], buffer insertion [7], bus encoding [8], and shielding [9], the fast methodology reduces the required simulation resource and eliminates the complexity of chip behaviors using the equalization (EQ) function in a pre-layout analysis. [10]

2. BOARD STACKUP AND MATERIAL SELECTION

The design of the board stackup is important in relation to signal integrity. Stackup is the arrangement of different layers between the substrate. Stackup is made up of the core, prepreg and copper foil. The core is a dielectric material with copper foil on both sides. Different cores are joined together by prepreg to form a stackup. The core has fix height dielectric but the prepreg can be adjusted. If the stackup is poorly designed then it can cause problems for signal transmission and SI issues such as crosstalk and EMC problems.

A stackup design helps the routing in signal layers with controlled impedance. The various layers are tightly packed with planes which help in the reduction of noise signals. The addition of planes in board causes a reduction in noise, such as crosstalk, and hence ensures a reliable transmission of the signal. In addition, it provides a stable voltage to the board. The stackup design involves the collaboration of a layout designer, hardware engineer, signal integrity engineer, and fabrication engineer.

There is a tradeoff between the signal reliability and cost factor. The following parameters affect the stackup design:

1. Selection of substrate material
2. PCB Layout
3. Number of power planes
4. Number of signal layers
5. Substrate thickness
6. Copper thickness
7. The arrangement of signal layers between planes and substrate

2.1 Material Selection and PCB Layout

Selecting the right material is important for the printed circuit boards. The base material used in PCB is made up of resign, reinforcement and a conductive foil. PCBs are used for various applications with different environmental conditions hence they require different materials according to the environment. The designers consider the physical, chemical, thermal, mechanical and electrical properties. The selection of the dielectric is important and usually flame retardant 4 (FR4) material is used. Prepreg is made up of a thin sheet of fiberglass impregnated with epoxy resign. The standard material must be used which is halogen free and without any hazardous materials. Material selection also depends on the vendor. Other material can also be used according to the design requirement but in this case, the cost factors must also be taken into account.

The type of materials used in constructing electronic circuits becomes more critical with the use of high frequency signals. The properties that most influence the signals are related to the conductivity, permittivity (εr) and dissipation factor (tan

δ) of the materials. Ideally, the conductors should have low a resistivity. In addition, the shape, width, and thickness of the conductor trace should be consistent throughout the circuit path. Conversely, the substrate materials should be fully insulating. The dielectric constant of the material should remain stable with increasing signal frequency. Through the selection of the right materials, the dissipation factor may be minimized. In terms of productivity, however, these material properties should be considered along with other characteristics such as material availability, process ability, and cost.

FR-4 materials have been the most successful and most commonly used materials in printed circuit manufacturing for many years. FR-4 actually encompasses a range of material types, although they share certain properties and are primarily epoxy based. The result is that there is typically an FR-4 material available for the most common end user applications. For relatively simple applications, the 130 to 140 ˚C FR-4s have become the material of choice. In higher-layer-count multilayer circuits and in very thick circuits, as well as in circuits requiring improved thermal properties, the 170 to 180 ˚C FR-4s have become the material of choice. In circuits requiring improved electrical properties, FR-4 materials with low dielectric constants and low loss properties are also available. The components used in FR-4 materials, particularly woven fiberglass cloth and epoxy resins, provide a very good combination of performance, process ability, and cost characteristics.

The layout describes the physical dimension of the board. This is decided according to the number of components used on the board and types of components such as through hole or surface mount. Placement of the components is also very important in the layout. The component placement must not violate the electrical trace length and propagation time delay. In addition, the digital circuitry must be separated from the analog circuitry, and any high frequency component which can affect the performance of other components must be isolated.

2.2 Power Planes and Signal Layers

The layer stackup power planes are designed first and then the signal layers. First, the number of power sources and their respective grounds are identified. The planes in the PCB help to reduce noise. They are also used for the return path of the signal. We define the plane first if the track width is large and there are a large number of traces to the route. Sometimes different power supplies have the same ground, in which case planes are defined accordingly. The power and ground planes should be adjacent. For isolation, it is recommended to add extra ground planes or if the total number of layers is odd, then extra ground plane should be added.

The number of layers in the PCB is directly related to the cost, as the greater the number of layers, then the higher the cast will be. If the density of routing tracks is equivalent to the number of layers, then the stackup will be cost effective. Too much addition of signal layers gives wide routing spacing and less crosstalk, but it makes the PCB thick and costly. Hence the number of signal layers is related to the routing density.

2.3 Arrangement of Signal Layers between Planes and Substrate

The arrangement of signal layers is also important. For every power plane, there should be a ground plane, and at high frequencies, it is recommended that both power and ground planes should be adjacent to attain the maximum capacitance between them. The signal layers are placed between two power ground plane pairs.

3. PCB PRE-LAYOUT ANALYSIS

The number of layers in the stack-up depends on the board, a number of routed signals, and power requirements. It is up to the designer to choose the number of layers on the board. All signal layers are separated from each other by ground or power planes.

We chose two reference boards and compared them with reference to their stackup. One is an old version and the second one is a new version with design modifications. The old board consists of 14 layers with a 1.6mm thickness and the new board is an 18 layer card. 10 layers are reserved for the power plane and the remaining 8 layers are for the signals layers. This board is 2.3mm thick. The stackup of the old board is shown in Figures 1 and 2 respectively. The thickness of the signal layer is shown in ounces (oZ) while the dielectric layer is in (mils). Where

1 inch = 1000mils

1 ounce = 1.35mils

1mil=0.0254mm

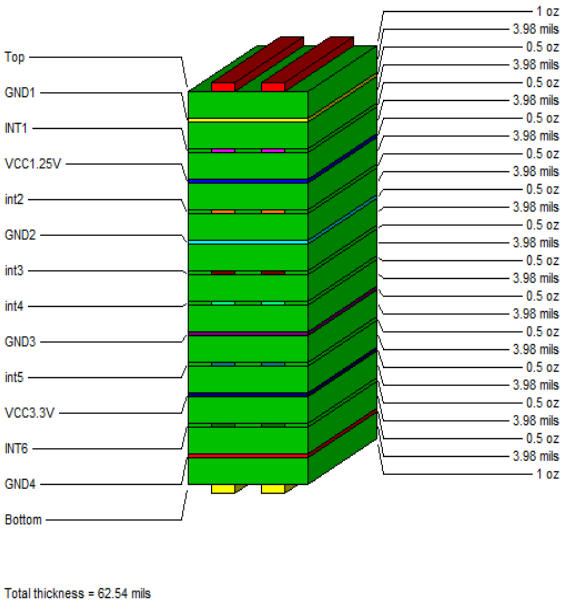

Figure1: Layout of the design

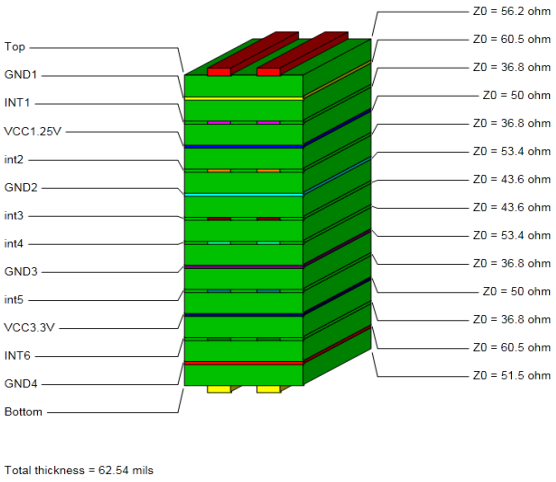

Figure 2: Layer stackup of the old board

In the old PCB, we had a problem with the video link signals. After a critical analysis, it was discovered that that this was due to an incorrect stackup. Appropriate grounding was not available for some signal layers.The video signals were without control impedance. The selected video signal in which the problem occurred is shown in Figure 3.

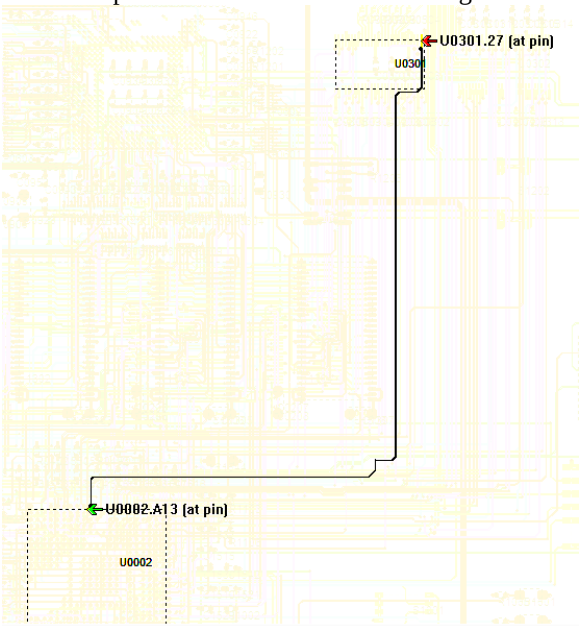

Figure 3: Video signal due to incorrect stackup

Analysis of video signals is done in Hyperlynx. The simulation of the selected net is shown in figure 4:

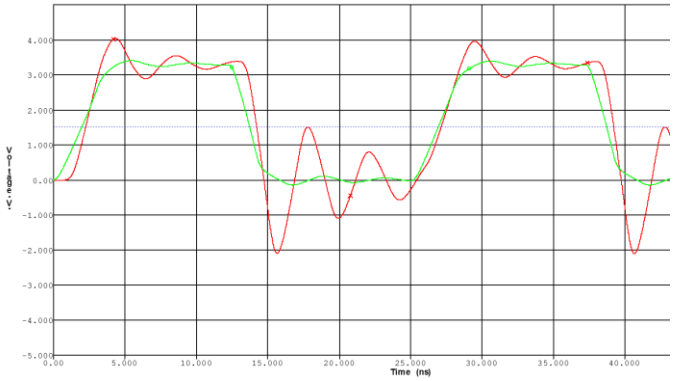

Figure 0: Both transmitted and received signals

The transmitted signal is green, while the received signal is shown red.

3.1 New Design and Discussion

In the new design, the stackup is planned with control impedance and with an increase in the number of layers from 14 to 18 and its thickness is increased from 1.6mm to 2.3mm. The Stackup in Hyperlynx is shown below in Figures 5 and 6 respectively.

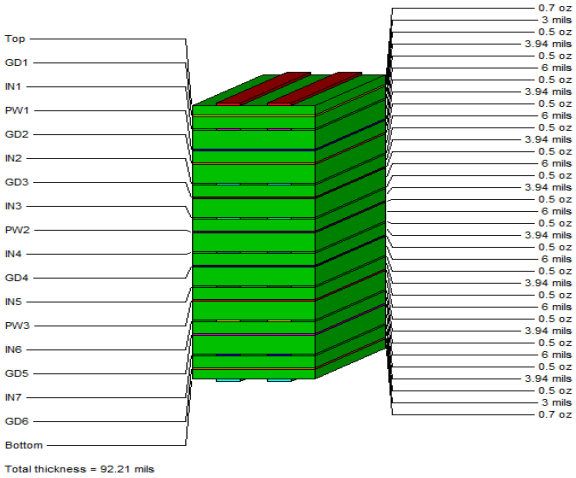

Figure 5: Layout of the new design

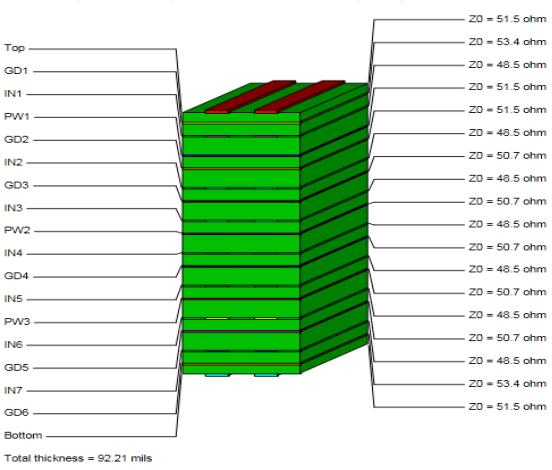

Figure 6: Stackup of the new board.

The selected signal is shown in Figure 7. Hyperlynx is used for analysis and simulation results.

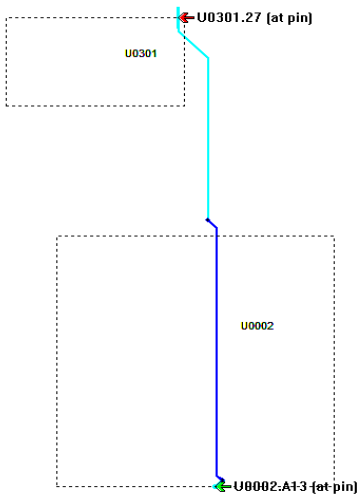

Figure 7: Selected signal from FPGA.

Transmitted blue signal and received red signal as shown below in Figure 8.

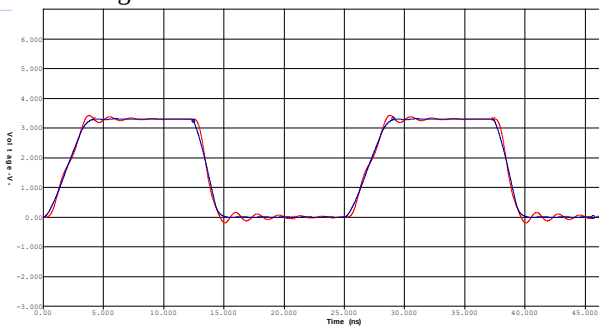

Figure 8: Both transmitted and received signals

Following Tables, I and II give a comparison of old and new boards.

Table I: Physical layout

PCB	Signal Layers	Power Planes	Ground Planes	Thickness (mm)
Old	08	02	04	1.6
New	09	03	06	2.3

Selected net comparison between old and new boards.

Table II: Comparison of old and new boards

Camera Link Signal	Effective net Zo (Ohms)	Positive Overshoot (mV)	Negative Overshoot (mV)
Old	34.5	913.5	1200
New	46.1	45.46	286.4

The comparisons above clearly shows good agreement to results as expected with control impedance by increasing the number of layers from 14 to 18 with the trade off in thickness from 1.6mm to 2.3mm.

4. CONCLUSIONS

The stackup is an important step in signal integrity pre-layout analysis. Here we compared our old and new pcb boards. The new board with 18 layers with a correct stackup and control impedance showed better results. While on the other hand, in the old board the stack was without control impedance and there was too much reflection in the camera link signal going to FPGA board.

5. REFERENCES

[1] J. Fan, X. Ye, J. Kim, etc., Signal Integrity Design for High-Speed Digital Circuits: Progress and Directions, *IEEE Trans. on Electromagnetic Compatibility*, **52(2)**, 392-400, **(2010).**

[2] B. P. Kamal, R. V. Paresh, Significant of Signal Integrity in High Speed Board Design, *International Journal for Scientific Research & Development, **2(4)**,571-573, **(2014).***

[3] R. T. Kushal, and P. P. Raymond, Signal Integrity Consideration in High Density, Boards, 10th International Conference on Electromagnetic Interference & Compatibility, 113-117, **(2008).**

[4] K. Xiao, B. Lee, X. Ye, A Flexible and efficient bit error rate simulation method for high-speed differential link analysis using time-domain interpolation and superposition, *IEEE International Symposium on Electromagnetic Compatibility*, 1-6, **(2008).**

[5] J. Zhang, E. G. Friedman, Effect of shield insertion on reducing crosstalk noise between coupled interconnects, *International Symposium On Circuits and Systems*, 529-532, **(2004).**

[6] M. Lampropoulos, B. M. Al-Hashimi, P. Rosinger, Minimization of crosstalk noise, delay and power using a modified bus invert technique. *Design, Automation and Test in Europe*, 1372-1373, **(2004).**

[7] E. Macii, M. Poncino, S. Salerno, Combining wire swapping and spacing for low-power deepsubmicron buses'. *ACM GLSVLSI*, 198-202, **(2003).**

[8] T. Zhang, S. S. Sapatnekar, Simultaneous shield and buffer insertion for crosstalk noise reduction in global routing, *IEEE Transaction on Very Large Scale Integration. (VLSI) System*, **15(6)**, 624–636, (**2007).**

[9] B. Victor, K. Keutzer 'Bus encoding to prevent crosstalk delay'. IEEE Int. Conf. on Computer-Aided Design, 57-63, **(2001).**

[10] H. Jimmy, S. Thonas,L. Yuan-Liang, H. Edward, X. Kai, Y. Xiaoning and W. Kai-bin, Fast Signal Integrity Methodology for PCB Pre-layout Analysis and Layout Quality Check, *63rd Electronic Components and Technology Conference*, 2012-2017, **(2013).**