NONLINEAR TRANSIENT CHARACTERIZATION OF THIRD ORDER VOLTAGE SWITCHED CP-PLL

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ABSTRACT: *The mixed signal PLL commonly know as CP-PLL is widely used in several Mobile and Wireless application. Due to hybrid nature it is very complex to analyze the system during off-locking. Linear approach is prefered to design the system, however linear approach is quit limited and valid only in the locked state. Furthermore, analysis of the higher order CP-PLLs become more complex. The PLL operating with VSCP-PLL is exhibits pecuiliar behavior in the form of aymmetrical pump current which impact the non-linear transient domain of system. Transistor level modeling is higly time and resource in efficient. Therefore to tackle all these issues like highly stochastic nature, mixed-signal behaviour, simultanous inclusion of high and low frequency parts in the loop, a fast and efficient modeling and simulation approach is necessary. Thus, in this paper an efficent Event Driven modeling approach for third order VSCP-PLL is derived. The developed model is validated using transistor level simulations and also compared with existing linear approach.* A fast, efficient and more accurate modeling technique is achieved.

Keywords: PLL, voltage switched charge pump, event driven modeling and simulation technique, non-linear switching behavior.

INTRODUCTION

The charge-pump phase locked loop (CP-PLL) is widely used subsystem in mobile and wireless communication, and smart system applications [1]-[3]. The CP-PLL is a heterogeneous system involving the co-design of the analog, digital and RF blocks [4]. This heterogeneity results in complicating the design and analysis of the CP-PLL systems. The CP-PLL is consist of several block connected in a loop as shown in Fig.1. This loop representation is mostly used in the frequency synthesis and tracking application [1]. The CP-PLLs are mostly used to track the ramping reference frequency in applications like Doppler shift [5]. The digital phase and frequency detector (PFD) block is a state machine usually realized by using the sequential circuits [6]. The PFD detects the phase error between two signals, i.e. reference signal and the feedback signal. The charge-pump provides a pulse width modulation correction signal based on the detected error signal. The LF suppress the noise and higher order harmonics of detected signal and provides a quasi-dc signal to tune the voltage controlled oscillator (VCO) [5]-[6]. A frequency divider circuit is realized in the feedback loop to perform the frequency synthesis function. Generally the CP-PLL used in applications like frequency synthesis and tracking application are operated by a current switched charge-pump (CSCP) [7]. This configuration of the charge-pump delivers a constant current during one switching cycle. The design of an ideal CSCP is challenging due to non-ideal effects that are inherent to PFD-CSCP transfer function. Furthermore, the conventional CMOS CSCP exhibits some non-ideal characteristics like mismatch, slew rated current pulses due to the commutation delay transferred from the PFD to the CSCP [8]. The pump current cannot set instantly to $\pm I_p$, since the actual current pulse is not perfect and

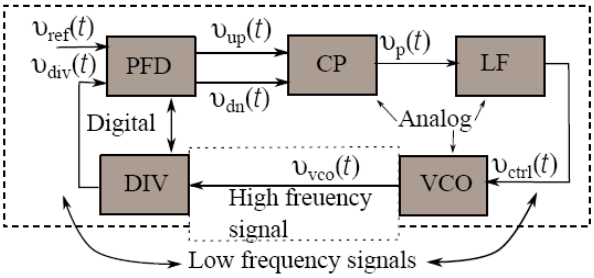

Fig. 1: The general representatopm of the CP-PLL system.

incorporates switching delay and slew rates, the phenomenon is illustrated in Fig. 2. These non-idealities influence the performance of the CP-PLL as a frequency synthesizer by increasing the spurs level in the output spectrum and influence the spurs level in the output spectrum and influence the transient characteristics (lock range, settling time) [7]. Because of these challenges, in some PLL chips a voltage switched charge-pump (VSCP) delivering a constant voltage during one sampling period (as shown in Fig. 3) is preferred [9]. The advantages of utilizing a VSCP are the cheap realization costs and the major aspect is related to the design simplicity of the VSCP structure [10]. However, a VSCP introduces a highly peculiar effect since the current during one sampling period is not constant [6],[9]. The variation in the pump current is related to the difference between the supply voltage (V_{DD}) and the initial voltage across the capacitor of the LF circuit . This peculiar effect produces asymmetrical dynamics, if the PLL is operating at $V_{DD}/2$ [11]. Therefore, different modeling approaches like linear modeling, behavioral modeling, transistor level modeling are used to characterize such a highly stochastic system[4]. Linear model can be used to

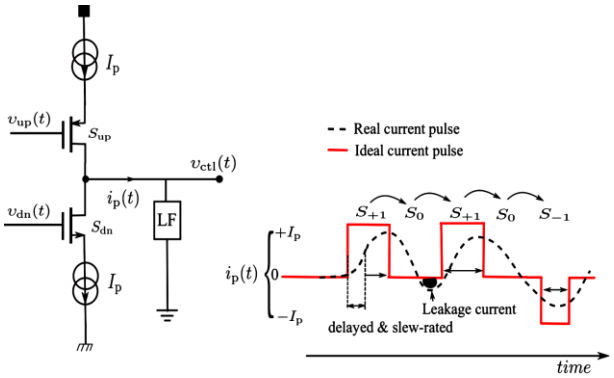

Fig. 2: Current switched charge pump and it ideal and real behavior output current pulse.

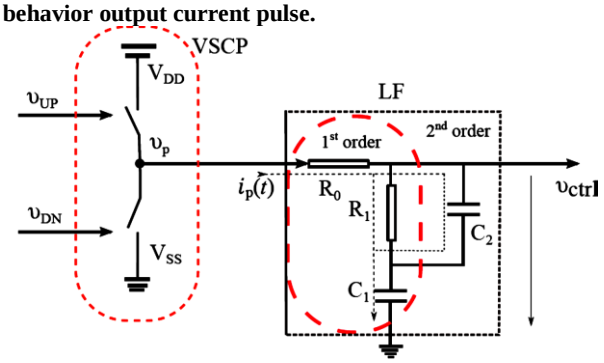

Fig. 3: The schematic of the VSCP and aitrary order LF.

predict the average behavior if the PLL when it is locked and considering two prior linearization of PFD and VCO circuit. Therefore, linear model cannot predict the non-linearities and non-idealities related to circuit level implementations of PLL[5]. Even though linear modeling provides an starting point considering the empirical design of the system. To model the more accurate system, the transistor level models accompanied with behavioral models are used to finalize the design process [10]. But these modeling and simulation approaches are highly time and computer resource inefficient. Therefore a more robust and efficient approaches is required. In the second step behavioral model is used to characterize the high level behavior of the system and then design process is finalized using transistor level simulations. If the robust design is not achieved then the conventional design process is repeated [12] until a satisfactory design is achieved. This cycle of redesign is highly time and resource costly. Therefore, a fast, efficient and more accurate methodology is necessary to characterize the non-linear switching behavior of mixed-signal PLL system. The Event Driven (ED) modeling technique presented in [13]-[18] is most efficient method than other linear method and transistor level models. This technique is has been mostly applied on PLL operating with a CSCP. However, still it need to be applied on most of the pulse width modulated system to characterize the mixed-signal behavior. In this paper we have applied ED model to the third order VSCP-PLL and results are compared with the linear theory and transistor level simulations.

VSCP-Architecture

The general CP-PLL functional blocks are shown in Fig.1. The major difference between the VSCP-PLL and the conventional CP-PLL is integration of a VSCP which necessitate the inclusion of a resistor between the VSCP and LF [1] as shown in Fig.3. Furthermore, when using second order LF to realize a third order PLL, it is essential to transform the lead-lag filter to represent high impedance state to depict the exact transient behavior of the system. The VSCP delivers voltages ($V_{DD,}$ υ_{ctrl} and V_{SS}) during UP, Zero and Down states of the PFD [5],[15]. Due to the difference of potential between the capacitors of the LF and the supplied pump voltage, a highly peculiar effect in the form of asymmetrical current exist which may affect the natural oscillation frequency of the system.

Event Driven Modeling Technique

The principle of phase locking of the mixed-signal PLL is basically dependent triggered nature of the PFD block [5]. The PFD reacting on the falling or rising edges, detects the phase error during the switching interval of the two consecutive events [14]-[16]. Where the phase error is actually the phase difference between the two falling (rising) edges. Thus, it is enough to calculate the instant these commutation edges as shown in Fig. 4.

The differential equation equations of the LF can be used to define the dynamic behavior of the loop between these switching instant. At the instant of falling edges, the phase of the reference signal having angular

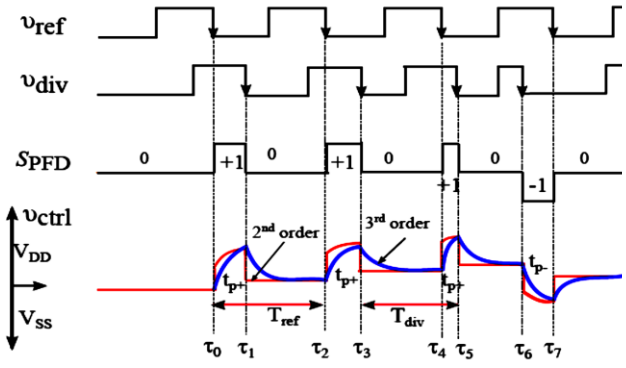

Fig. 4: The concept of the Event driven methodology

freqeuncy ω_{ref} can be calculated as:

$$\varphi_{ref}(t_{n+1}^{ref}) = \varphi_{ref}(t_n) + \int_{t_n}^{t_{n+1}^{ref}} \omega_{ref}(\tau)d\tau = 2\pi \qquad (1)$$

and phase of the divider signal having angular ω_{div} can be calculated as:

$$\varphi_{\mathrm{div}}\left(t_{n+1}^{\mathrm{div}}\right) = \varphi_{\mathrm{div}}(t_n) + \int_{t_n}^{t_{n+1}^{\mathrm{div}}} \omega_{\mathrm{div}}(\upsilon_{\mathrm{ctrl}}(\tau))d\tau = 2\pi \quad (2)$$

The falling events occur when phases of both signals is 2π. The falling instant of reference signal (t_{n+1}^{ref}) can be calculated analytically by solving the relation (1).

$$\varphi_{\mathrm{div}}\left(t_{n+1}^{\mathrm{ref}}\right) = \varphi_{\mathrm{ref}}(t_n) + 2\pi f_{\mathrm{ref}}(t_{n+1} - t_n) \quad (3)$$

$$t_{n+1}^{\mathrm{ref}} = t_n + \frac{(2\pi - \varphi_{\mathrm{ref}}(t_n))}{2\pi f_{\mathrm{ref}}} \quad (4)$$

Between two falling edges, the voltage pump signal modulates the internal dynamic state of the system. The tuning voltage of the VCO (υ_{ctrl}) is the key parameter to be determined between the successive triggering edges. The control voltage can obtained using state space representation of LF circuit.

$$\begin{aligned} \dot{x}(t) &= Ax(t) + B\upsilon_{\mathrm{p}}(t) \\ \upsilon_{\mathrm{ctl}} &= C^T x(t) + D\upsilon_{\mathrm{p}}(t) \end{aligned} \quad (5)$$

The ***x(t)*** represents the internal state of the system (i.e. the voltage across capacitors $\upsilon_{C1}(t)$ and $\upsilon_{C2}(t)$ of the LF), which then can be define by following solution:

$$x(t) = \Phi(t - t_n)x(t_n) + \int_{t_n}^{t} \Phi(t - \tau)\boldsymbol{b}\, \upsilon_p(t)d\tau \quad (6)$$

The generalized control voltage expression can represented as:

$$\upsilon_{\mathrm{ctl}}(t) = C^{\mathrm{T}}\left[\Phi(t - t_n)x(t_n) + \int_{t_n}^{t} \Phi(t - \tau)B\upsilon_{\mathrm{p}}(t)\right] + D\upsilon_{\mathrm{p}}(t) \quad (7)$$

By putting Eq. (7) in Eq. (2) and solving it, the phase relation of the divider signal can be obtained as:

$$\varphi_{\mathrm{div}}(t_{n+1}) = \varphi_{\mathrm{div}}(t_n) + \frac{2\pi}{N}\int_{t_n}^{t_{n+1}} \left[K_{\mathrm{v}} \left\{ \begin{Bmatrix} C^T \begin{bmatrix} \Phi(t - t_n)x(t_n) + \\ \int_{t_n}^{t} \Phi(t - \tau)B\upsilon_{\mathrm{p}}(t)\, d\tau \end{bmatrix} \end{Bmatrix} + f_{\mathrm{v},\phi} \right\} + D\upsilon_{\mathrm{p}}(t) \right] d\tau \quad (8)$$

Equation (8) is non-bijective one. which cannot be solved analytically but numerically. There are several numerical method (e.g. secant method) which can be used to estimate the time of the occurrence of edge of the divider signal (t_{n+1}^{div}) [12]. After calculating the event time of both reference and divider signal. The effective event impacting the loop dynamics is then obtained using the minimum operation:

$$t_{n+1} = \min\left(t_{n+1}^{\mathrm{ref}}, t_{n+1}^{\mathrm{div}}\right) \quad (9)$$

Determining the next effective triggering event at $\boldsymbol{t}_{n+1}$ from (9), then all state variable within a state matrix (M_{n+1}) can be calculated at the same time instant and then can be saved as initial condition to determine the next time instant:

$$M_{n+1} = \begin{bmatrix} t_{n+1} \\ \varphi_{\mathrm{ref}}(t_{n+1}) \\ \varphi_{\mathrm{div}}(t_{n+1}) \\ \varphi_{\mathrm{err}}(t_{n+1}) \\ \boldsymbol{x}(t_{n+1}) \end{bmatrix} \quad (10)$$

To simulate the derived Event Driven model an algorithm defined in [11]-[12] can be used, where all state variables in a state variable matrix (10) can be calculated in an iterative process.

SIMULATION RESULTS

To validate the derived Event Driven model, a transistor level model was designed in CMOS 130nm technology. The design of the VSCP and second order LF circuit is given in [1]. The current starved ring VCO [8] utilized here is based on 11 delay cells and having center frequency of 48MHz with non-linear transfer characteristics and K_{v} = 112.476 MHz/V is the gain in the small quasi-linear range. The divider ratio is 48. All the components of VSCP-PLL were designed and tested invidually and then simulations were performed by connecting them in the loop. The validation process can be defined as: first the transistor level model was simulated in Virtusuo (**Spectre**) simulator and then cotnrol voltage was extracted from the **Spectre** to **MATLAB**. Event Driven simulation were performed setting the same initial conditions and parameters.

A: Electrical Vs. ED-Model

The electrical simulation parameters and nearly the similar initial conditions are applied to perform ED simulations. It can be seen that, Fig. 6 both behavior are similar from its acquisition range to settling behavior of the system. The Event Driven model took 0.5 sec to obtain the 200us transient behavior, whereas the Spectre simulations took 5 hours to finish the transistor level simulations. This experiment shows that Event Driven model is more efficient in terms of speed and accuracy of the CP-PLL system simulation.

B. Linear approach Vs. ED Model

To validate linear model of the VSCP-PLL, it is necessary to approximate the non-constant pump current as quasi-constant and replacing voltage switched system by its equivalent current switched CP-PLL [6,9]. This linear model [6] for this typical architecture is only valid when PLL is locked at center frequency of the VCO and having a symmetrical dynamics (i.e. same currents in the up and down half cycle) [12].

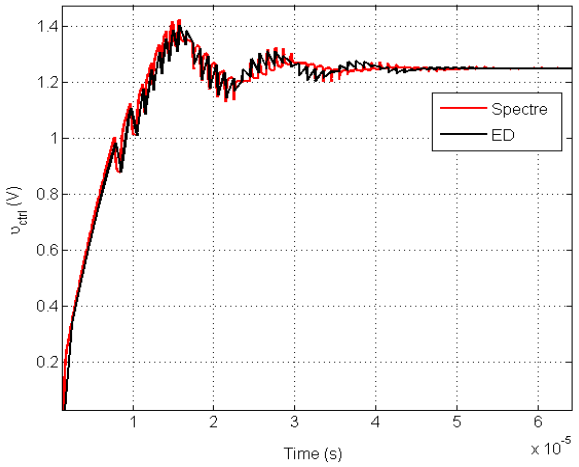

Fig. 5: Electrical and ED simulation of the third order VSCP-PLL. (Para: Ref: frequency =1 MHz, N = 48, R_0 = 80KΩ, , R_1 = 5KΩ, C_1 = 300pF, C_2 = 27pF, V_{DD}=2.5, V_{SS} = 0, Process = TT)

$$\omega_n = \sqrt{\frac{K_{v,\omega}K_d}{NC_1}} \quad \zeta = \frac{\tau_1}{2}\omega_n \quad K_d = \frac{I_p}{2\pi} \quad K_{v,\omega} = 2\pi K_v \tag{11}$$

This experiment shows that, the linear model can predict the average behavior of the system but only in the locked state. The Event driven model can predict the locked and unlocked conditions and it can expose the switching behavior tuning voltage more accurately.

CONCLUSION

A non-linear Event Driven model of third order VSCP-PLL has been presented. The Event Driven model has achieved both speed and accuracy to represent the actual behavior of the mixed-signal PLL. It has been shown that linear model is not very accurate and is limited to the locked condition of the system. The Event Driven model simulation achieves an speed factor of

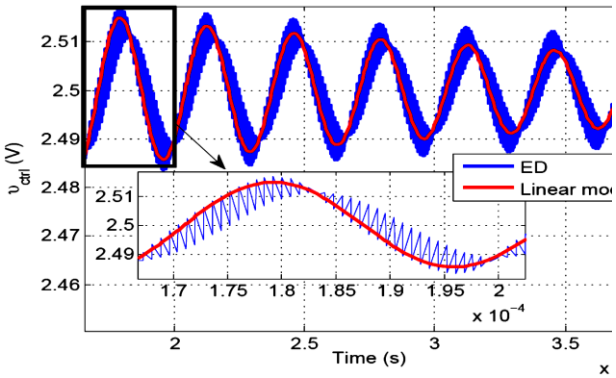

Fig. 6: Linear [6] and Event driven simulations of 3rd order VSCP-PLL (Parameters: K_v=2MHz/V, ζ =0.308, ω_n= 39.765 K rad/s, V_{DD} =5V, υ_{ctrl}=2.5V, $\Delta\upsilon_{ctrl}$ =0.2V).

36,000 comparing the transistor level simulations. The Event Driven can be extended to arbitrary ordered VSCP-PLLs to achieve a fast, resource efficient and more accurate design.

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