A NOVEL HIGH RESOLUTION VERNIER TDC, BASED ON MULTI-PATH GATED RING OSCILLATOR

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ABSTRACT: *In this paper an 11-bit novel Vernier Time-to-Digital Converter (VTDC) with high resolution; 4-ps, is presented for All Digital Frequency Synthesizer (ADFS). Using a multi-path gated ring oscillator at this work has demonstrated first-order noise shaping characters. The proposed TDC achieves fine time resolution (4-ps), large detectable range (11-bit), shaped high frequency noise, and low power consumption simultaneously. The VTDC architecture has been realized using digital gates and arbiter circuits to measure the time interval. The proposed VTDC is portable and scalable in other process technologies. Proposed VTDC has been simulated in 180nm CMOS and its consumption power is 1.5 to 16.5-mW from a 1.5 V supply, depending on the time difference between input edges.*

Keywords: Time-to-Digital Converter, Vernier TDC, high resolution VTDC, Gated Ring Oscillator, first order noise shaping, arbiter.

INTRODUCTION

Wireless communication has grown exponentially, with wide range of applications which offer for the customers. The over-increasing demands and continuously expanding markets for wireless communication systems have increased research in new architectures for improving quality, low power and reducing cost. The aggressive cost and power reductions of high-volume mobile wireless solutions can be only realistically achieved by the highest level of integration, and this favors a digitally intensive approach to conventional RF functions in the most advanced deep-submicron process.

As technology advances, on-chip clock multiplication becomes a necessity for most digital Integrated Circuits (ICs). A typical approach to achieve such clock multiplication is to employ a phase locked loop (PLL) circuit consisting of a phase detector, analog loop filter, frequency divider, and Voltage-Controlled Oscillator (VCO). Unfortunately, the analog component of PLLs prevents the advantages of typical digital design [1]. However, the conventional PLLs need the analog passive loop filter, which may occupy a large active area. Also they need analog charge pumps; these are sensitive to leakage current in deep-submicron CMOS processes. So these PLLs could not satisfy all wireless standard requirements.

Nowadays, All Digital Frequency Synthesizer (ADFS) envelop the conventional PLL characteristics and usually do not need any analog component. Fig. 1 shows a Digital Phase Locked Loop (DPLL) in the form of a fractional frequency synthesizer, in which a TDC has been used instead of traditional Phase/Frequency Detector (PFD) and charge pump. Its main advantage is removing the analog components of conventional PLLs. In the past few years ADFS, demonstrating its ability in wireless communication, has become a special research topic [2].

In ADFS, due to requirement of precise control or alignment of timing signals, the TDC is a fundamental block. It bridges the gap between the continuous-time analog

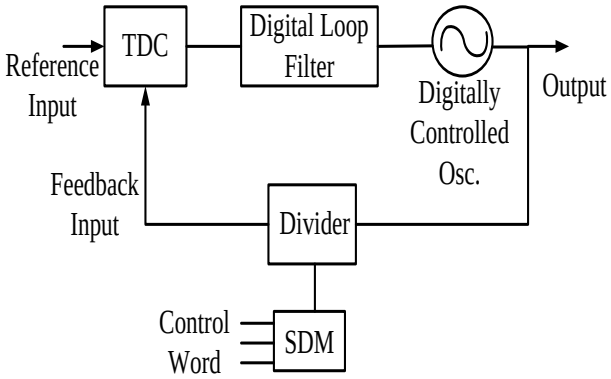


Figure 1. All Digital Frequency Synthesizer

domain and discrete-time digital domain. Achieving high performance in such systems depends on their TDC performance [3], which is used to measure the instantaneous time difference between the edges of feedback output and reference input.

As known, noise reduction is a significant point for increasing the transmission bit-rates, with acceptable bit-error rates [4]. The noise performance of a synthesizer is most often characterized by phase noise, which is a measure of the spectral purity of the system output. Despite this handicap, it has been studied in some literatures and it is an active research area, now [3, 4]. Synthesizer phase noise degrades the quality of transmission by folding other frequencies into the desired band. Due to TDC finite resolution, it introduces quantization noise on the output of synthesizer spectrum.

Some structures and techniques were presented to increase the TDC time resolution in literatures based on Vernier delay line structure [5, 6] and noise shaping technique [3, 7]. In [5], The TDC core consists of inverters and flip-flops. Its resolution equals intrinsic inverter propagation delay of 15–20-ps. In [6], the TDC time resolution is 8ps; it is clear that during the digitization of the input time interval, these resolutions inevitably generate large quantization noise in desired band. Also in [6], the delay of each stage depends on the amount of Vctrl and Vbias and Low reference clock is another difficulty for using this TDC in a ADFS. In [3, 7] a multi-path gated ring oscillator (GRO) was proposed to

improve the TDC resolution by noise shaping technique. But using more multi-path delay stages (47 stages) in this GRO increases its power consumption up to 21mW. Another big handicap in this architecture is using more than 100 up/down counters for time interval measuring.

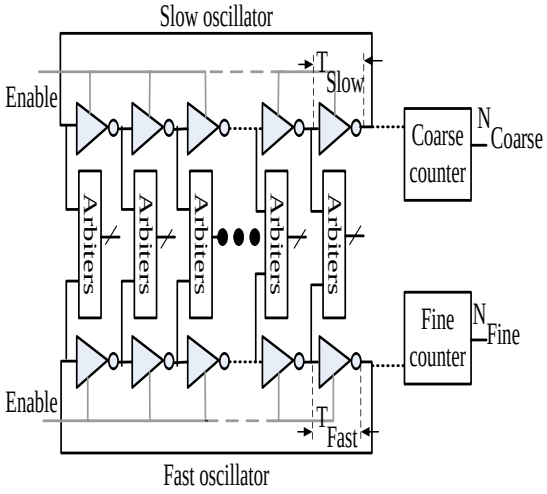
In this paper, motivated by the above problems, we present a novel high resolution Vernier TDC based on multi-path gated ring oscillator for wireless communication, where it utilizes Vernier TDC to increase the time resolution and Gate Ring Oscillator (GRO) for first order noise shaping.

This paper is organized as follows; the architecture design of proposed VTDC is presented in section 2; in this part we exhibit a fundamental block of proposed VTDC in order to explain its ability to perform noise shaping with an entirely digital component. In section 3 the simulation results and a comparison with other works are presented. Finally, a conclusion is depicted in section 4.

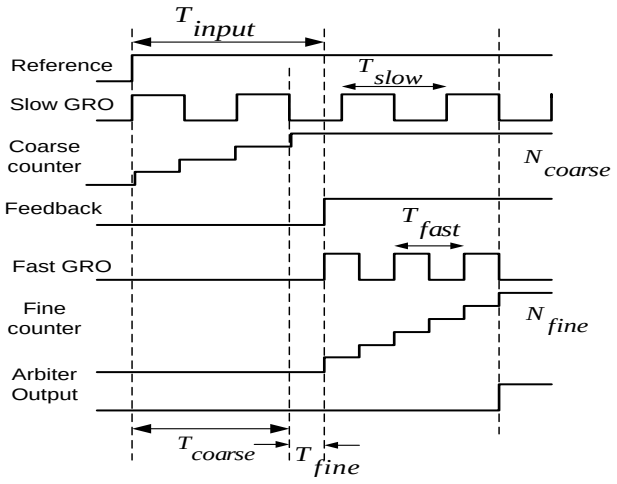
ARCHITECTURE DESIGN

Background

Generally in VTDC, two rings of inverters with slightly different delays are used to digitalize the difference of time interval between reference clock and feedback output. The goal of TDC is to measure the time difference between the rising-edges of the 'Reference' and 'Feedback' signals, as shown in Fig. 2. By asserting the 'Reference' signal, Enslow is activated; then the slow ring starts to oscillate with a period of 2NTslow and the number of oscillations is counted by the coarse counter. By asserting the 'Feedback' signal, after an input delay (Tinput), Enfast is activated; then the faster ring starts to oscillate with a period of 2NTfast and the number of oscillations is counted by the fine counter. Also by asserting the 'Feedback' signal, the coarse counter is disabled, and the output of the counter represents a coarse measurement of the time between 'Reference' and 'Feedback' rising-edges (Tcoarse).



(a)



(b)

Figure 2. Illustration of VTDC, (a) basic Vernier topology (b) timing diagram

Typically, to improve the measurement accuracy, the residue of input delay (Tfine) is measured by the Vernier structure. Since (Tfast) is smaller than (Tslow), the time difference between rising edges of two oscillators is reduced every cycle; thus the edge of fast oscillator eventually catches up the edge of slow oscillator and is detected by arbiter circuits. (Tinput) is determined as follows [8]:

$$T_{input} = T_{Reference} - T_{Feedback} \quad (1)$$

$$T_{input} = T_{coarse} + T_{fine} = N_{coarse} T_{slow} + [N_{fine} (T_{slow} - T_{fast}] \quad (2)$$

Where Nslow and Nfast are the number of slow and fast oscillator cycles until catch up time, respectively. Equation (2) represents the coarse and fine steps resolutions depends on the slow period (Tslow) and the difference of two oscillators' periods (Tslow – Tfast), respectively. As observed its effective resolution will improve by reduction of each stage delay; an effective resolution helps us achieve a low phase noise and fast locking time in ADFS. In fine step decreasing the Tslow – Tfast, is achievable by slightly different delays in two rings of oscillators. Since in VTDC key challenges are coarse and fine steps resolution; in current work to improve them, we used multi-path technique for oscillators and noise shaping technique, respectively.

2.2 Gated Ring Oscillator

Fig. 3 exhibits two implementation methods of Gated Ring Oscillator (GRO). In these oscillators, when Enable= '1', the inverter ring is oscillated and when Enable= '0', it suspends. In the conventional GRO, the input of each delay stage (V_{ini}), connects only to the output of previous delay stage ($V_{out\ i-1}$); so an achievable delay per stage in 180nm CMOS is about 22ps. In Multi-path GRO beside the input of each stage connection to the output of previous stage, it connects to the output of two other stages {$V_{out\ (i-j1)}$, $V_{out\ (i-j2)}$, $V_{out\ (i-jr)}$, where the difference of i and jr must be even}.

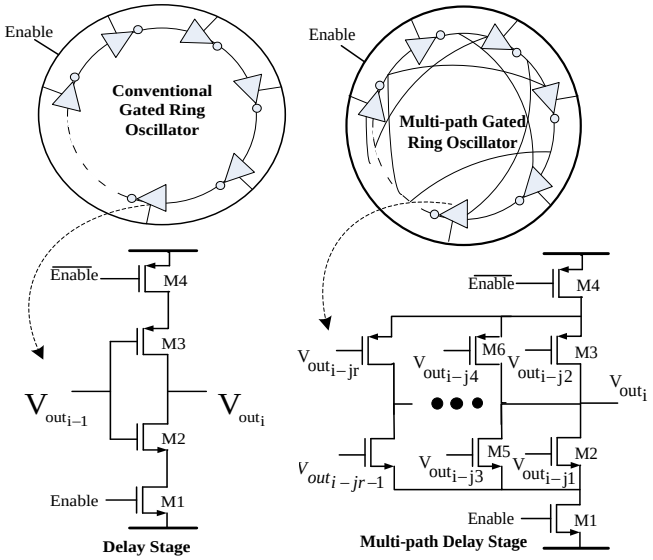
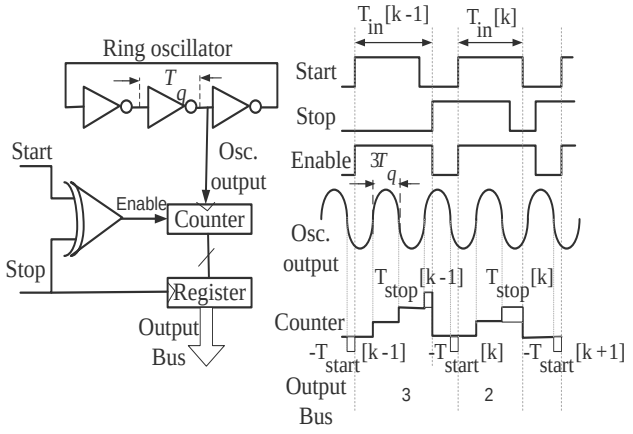


Fig. 3. Conventional versus multipath GRO and their delay stages

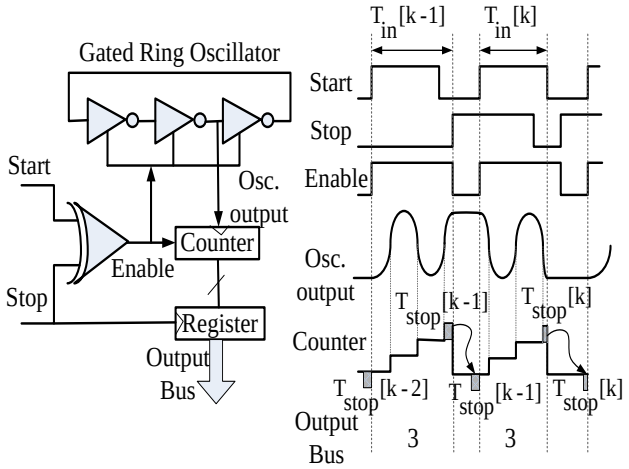
The main advantage of GRO over traditional ring oscillators is that the residue occurring at the end of every given measurement interval is transferred to the next measurement interval. This advantage lets us to do first-order noise shaping in TDCs. For more discussion, we represent two types of TDC in next section: specifically Classical TDC and Noise shaped TDC.

Classical architecture of TDC

Fig. 4(a) shows a classical TDC, which includes a traditional ring oscillator [3]. In this structure the oscillator transitions are counted during the Tin. Also the amount of counter is reloaded in register and resets when the Enable signal is low.



(a)



(b)

Figure 4. Ring oscillator-based TDC (a) Classical architecture, **(b) With noise shaping architecture**

$$Terror[k] = Tstop[k] - Tstart[k] \quad (3)$$

Tstart and Tstop denote the times at the beginning and end of the Enable signal. This error can be decreased using a GRO which is caused by noise shaping technique.

Noise shaping architecture of TDC

Figure 4(b) illustrates the concept of noise shaping technique in the TDC. As aforementioned, in this structure when Enable signal fall to Low, the oscillator suspend its amount until next raising edge of Enable signal. By preserving the oscillator state at the end of the measurement interval Tin[k-1], the quantization error Tstop[k − 1] from that measurement is also preserved. In fact, when the following measurement of Tin[k] is started, the previous quantization error is carried over as Tstart[k] = Tstop[k−1]. This results in first-order noise shaping of the quantization error in the frequency domain, as evidenced by the first-order difference operation on Tstop. Therefore the measurement error is given by:

$$Tstar[k] = Tstop[k-1] \quad (4)$$

$$Terror[k] = Tstop[k] – Tstart[k] \quad (5)$$

Therefore;

$$Terror[k] = Tstop[k] – Tstop[k-1] \quad (6)$$

$$Terror[k] = (1- z^{-1}) Tstop[k] \quad (7)$$

Equation (7) indicates a first-order noise shaping (pushed to high-frequency) in the frequency domain. In summary, noise shaping can be achieved by using a GRO topology in TDC, where shaped noise can be mitigated by digital filter in ADFS.

PROPOSED VTDC

The proposed TDC architecture for a Vernier TDC is shown in Fig. 5. This VTDC consists of three major blocks, namely: Multi-path Gated Ring Oscillator, pre-logic and Evaluation logic units.

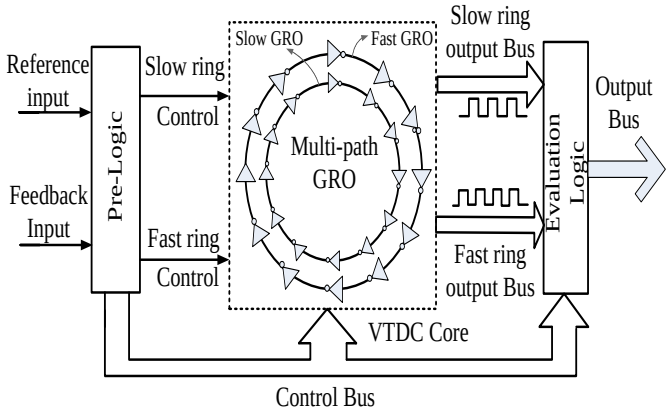


Figure 5. Block diagram of proposed VTDC

The proposed VTDC has been inspired from the conventional VTDC, presented in [6], with some differences. The first difference of this work is that inverters were used as the multi-path gated stages to construct the VTDC in a standard digital process and the second is using noise shaping technique. Fig. 2(a) illustrates the concept of the proposed VTDC core.

The VTDC core consists of two arbiter chains as illustrated in Fig. 2(a); each arbiter compares the edges of GROs signals. Fig. 6 shows the schematics of proposed arbiters. The arbiters need to be reset at each judge before the next comparison starts; so reset circuit (forms by M7 and M8) is utilized in its core. Rising and falling edges of slow and fast GRO fed into the arbiters. An arbiter judges whether the reference catches up to the feedback or vice versa. In catch up the stop bit of arbiters set to "1" and this bit controls the fine and coarse counters. Rising and falling edge detectors are shown in Fig. 7.

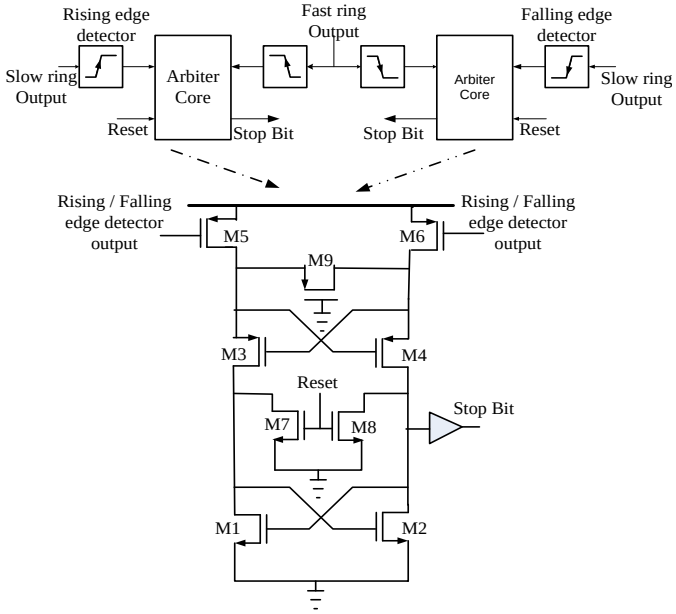


Figure 6. Circuits of arbiters

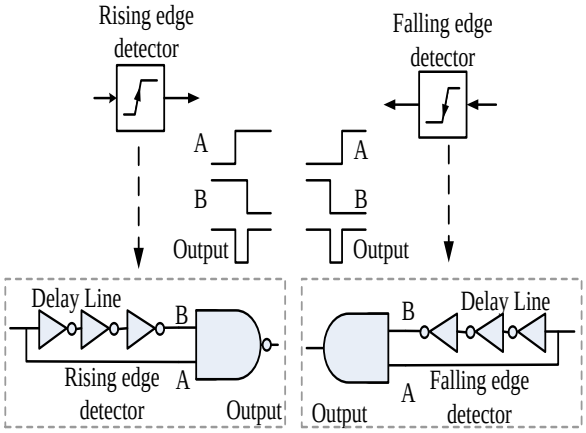


Figure 7. Rising and falling edge detectors

The pre-logic unit is the critical building blocks of VTDC. In ADFS the reference signal may lead or lag the feedback signal. Therefore for proper functioning of VTDC the slow GRO must start to oscillate before the fast GRO. Otherwise, VTDC will not work [6]. As displayed in Fig. 8, the pre-logic unit consists of delay lines, an arbiter, and two multiplexers (MUX). The delay of buffer lines must be adequate to compensate for the propagation delay of arbiter path and MUX switching. The output of arbiter, named with sign bit, will be "1" when the feedback signal leads to the reference signal. Otherwise the sign bit will be "0". This sign bit represents the positive and negative phase error in ADFS.

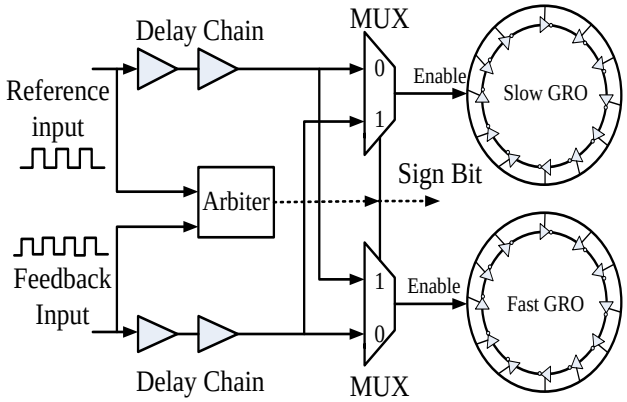


Figure 8. Pre-logic unit

The Evaluation block in Fig. 5 consists of calculation logic and a register bank, as shown in Fig. 9. Calculation logic and register bank are used to estimate the equation (2) and hold the amount of control/output bus, respectively. For time interval measuring, the calculation logic with respect to the amount of fine and coarse counters estimates equation (2), and then sends it for register bank. By triggering the read pulse, the register bank transfers the calculated digital words into the control bus and output bus.

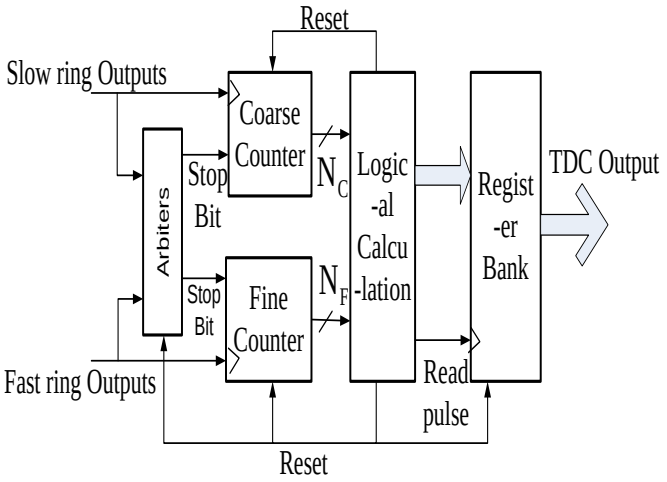


Figure 9. Evaluation block diagram

SIMULATION RESULTS AND DISCUSSION

The proposed VTDC was simulated by RF-Hspice with 180nm RF-CMOS technology. The simulation results were carried out by using FRef = 40MHz as reference frequency.

The power consumption of proposed VTDC is a linear function of enable signal width, corresponding to its inputs time interval. Simulation results show the consumption power ranges 1.5 mW to 16.5 mW from 1.5V supply voltage. Since higher supply voltage arrives to a shorter delay and increase the power consumption. In this work we achieved a best tradeoff between the power consumption and resolution time with 1.5V supply voltage. At this voltage, the time resolution of the proposed VTDC (bin size or 1 LSB) is 4-ps. This result verifies the significant benefit in time resolution.

The achieved resolution of 4-ps represents an improvement factor of over 7 compared to a classical TDC resolution of 30-35-ps under the same voltage supply and operating conditions [9].

This VTDC was employed in the ADFS. The carrier frequency which came from the ADFS was FCarrier = 3.6-4 GHz. So the frequency of feedback signal, which is one of the VTDC inputs (as shown in Fig. 1), can be concluded as follows:

$$FFeedback = Fcarrier / NDiv \quad (8)$$

The proposed VTDC transfer function versus an ideal TDC transfer function, over the entire dynamic range is shown in Fig. 10. The difference of these two transfer function presents VTDC timing/conversion error. To obtain the transfer function, the frequency division ratio, NDiv, must be changed slightly to experience slow edge rotation in Freference and FFeedback. The VTDC output code is averaged over 20 cycles to eliminate chatter. The simulation results show that the conversion error is less than 1 LSB and the timing error is nearly ideal.

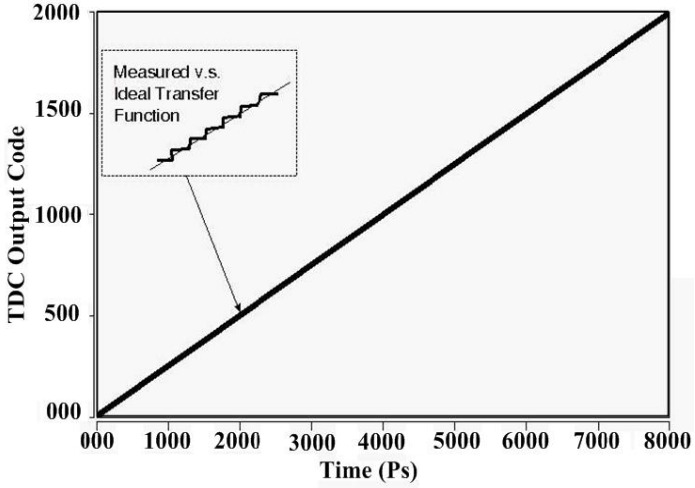


Figure 10. Measured versus ideal transfer function

To simulate the noise shaping in Fig. 5, first two input frequencies with small difference, where the difference includes an offset time and a sinusoid time changing, are applied to the Reference and Feedback and then FFT is taken from the output code. In this test, we applied a 40 MHz to reference and a 40 MHz addition to 1ns offset and a 100 kHz input of 2-pspp. Fig. 11 shows the time domain VTDC output code. Fig. 12 and Fig. 13 display the simulation results of output code FFTs for without and with first order noise shaping states, respectively.

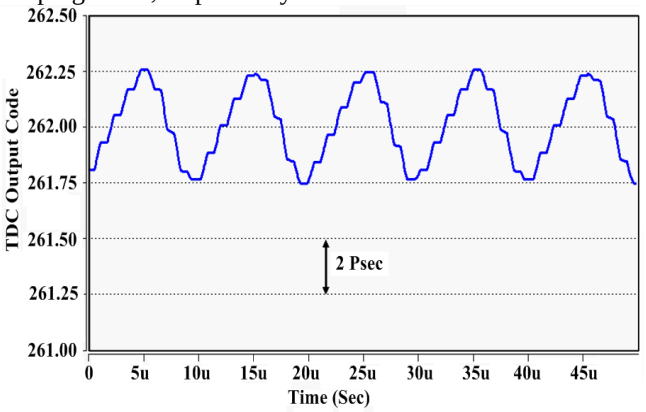


Figure 11. VTDC output with sinusoidal delay sweep 2-ps (p-p)

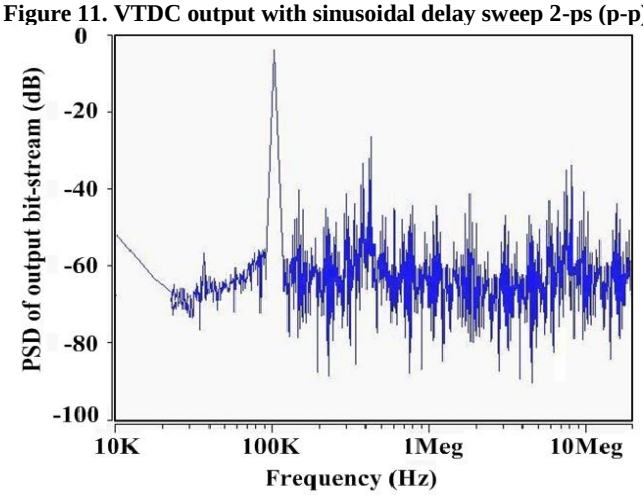


Figure 12. Power spectral density in the frequency domain for delay sweep 2 ps (p-p) without first order noise shaping

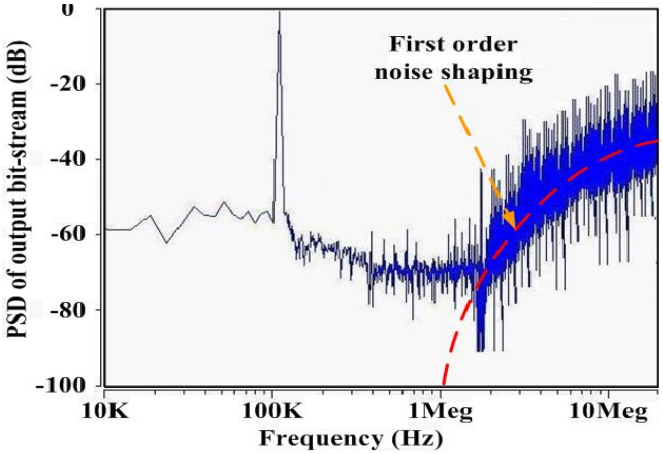


Figure 13. Power spectral density in the frequency domain for delay sweep 2 ps (p-p) with first order noise shaping

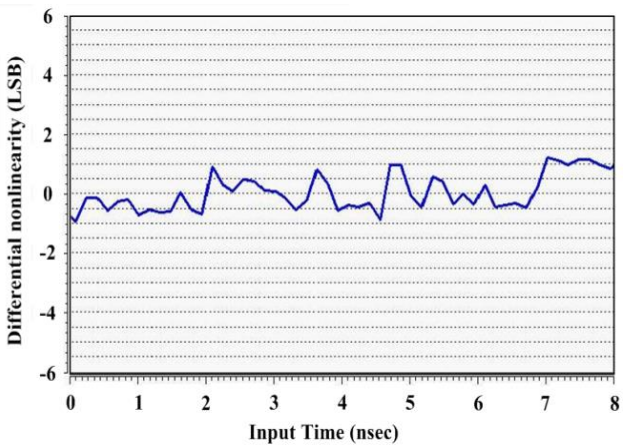


Figure 14. Differential nonlinearity performance of VTDC

For a classic Vernier TDC simulation results indicate that the quantization noise has a "white" noise floor. Also, as illustrated in Fig. 13, in the proposed VTDC, most of the quantization noise is pushed to high-frequency region and the in band noise level degrades more than 10dB. Simulated results have very good agreement with the theoretical first-order noise-shaping. When this proposed VTDC is utilized in the ADFS, shaped high frequency noise can be digitally filtered by digital low pass filter which is implemented in the ADFS.

As exhibited in Fig. 14, the linearity of proposed VTDC was measured by DNL test as presented in [13], from 0-ps to 8-ns time interval with 4-ps steps. This test was performed 100000 times, 50 sample per each step. Simulation result shows that the nonlinearity of designed VTDC is less than ±4-ps (1LSB) for 0-ps to 8-ns time intervals. Therefore the DNL test emphasizes that a variation in the input time interval of VTDC has a minimal impact on the precision of the VTDC.

Table I shows a detailed comparison between this work and other TDC realizations. This table illustrates that proposed VTDC has a better performance compared to similar devices, especially achieving high resolution below 4-ps within 11bit dynamic range. Of course it must be noted that the power dissipation depends on the input time interval, and it increases with time interval increasing.

CONCLUSION

In this paper, we have designed and analyzed a novel VTDC with high resolution for ADFS. The proposed VTDC has an 11bit dynamic range and 4-ps LSB. The linearity test result indicates that the VTDC sustains a DNL under 1LSB.

Using a multi-path gated ring oscillator at current work led us to apply first-order noise shaping. Using first order noise-shaping techniques resulted good resolution in designed VTDC beside of decreasing in-band noise. In this case, the fundamental ability of this VTDC to perform time interval digitalization with highly digital circuitry was observed to efficiently achieve high-performance ADFS in advanced CMOS technology.

Table I. Comparison to previous work

Reference	[6]	[2]	[10]	[11]	[12]	This work
Clock frequency	15MHz	50MHz	100MHz	40MHz	150MHz	**40MHz**
Time Resolution (ps)	8	6	97.5	250	24	**4**
Dynamic range (bits)	11	12	8	12	N.A.	**11**
DNL	N.A.	N.A.	±0.3LSB	±0.8LSB	N.A.	**<1 LSB**
Noise shaping	No	Yes	No	No	No	**Yes**
Supply Voltage	1.5v	1.5v	5v	3.3v	N.A.	**1.5v**
Power Dissipation	7.5mW	2.2-21mW	175mW	50mW	50mW	**1.5-16.5mW**
Cmos Process	130nm	130nm	500nm	500nm	350nm	**180nm**

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