A NON-ISOLATED INTERLEAVED HIGH STEP-UP SWITCHED-CAPACITOR CONVERTER FOR DISTRIBUTED GENERATION SYSTEM

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***ABSTRACT**: A non-isolated interleaved boost converter with coupled inductors and switched-capacitor circuits is presented in this paper, which can be employed for renewable energy conversion systems including the photovoltaic (PV) and the fuel cell (FC). Whereas the voltage generated by these sources is low, a converter with high voltage conversion ratio is the main requirement for connection to a relatively high dc-bus voltage. To obviate this necessity, a switched-capacitor circuit is magnetically connected to interleaved boost converter, which effectively increases the voltage growth and decreases the voltage stress in the semiconductor components, and thereby, the conduction losses are diminished. In fact, the proposed converter operates as a flyback converter in some times and forward converter in other times. To restrain the leakage energy of the coupled inductors and confine the voltage spikes on the main switches, the active clamp technique is employed. Furthermore, the zero voltage switching (ZVS) operation is guaranteed even in the light load, which leads to degradation of the switching losses. Also, the leakage inductance of the coupled inductors is handled to realize zero-current-switching (ZCS) performance of the diodes. At last, a 1-kW prototype is implemented to confirm the theoretical analysis and performance of the proposed topology.*

Keywords: Active clamp circuit; coupled inductor; high step-up converter; interleaved boost converter; switched-capacitor

LIST OF SYMBOLS

C	capacitor
L	inductor
I	current
R	resistor
t	time
V	voltage
ZCS	zero current switching
ZVS	zero voltage switching

1. INTRODUCTION

To solve energy problems as rapidly rising fossil fuels costs and environmental deterioration, employing renewable energy sources including photovoltaic (PV), fuel cell (FC), wave, as a major form of clean technology could be the benefit solution [1,2]. Between these sources, system based PV and FC power are appropriate sources for the future energy challenge because of their significant merits as high efficiency, low environmental impact and more reliable generated power [3,4]. But, relative low output voltage is the main defect of these energy sources, therefore, existence of a converter with high voltage gain is essential to regulate and lift their output voltage to a higher level for grid connected application [5, 6]. It is important, therefore, to discover and evaluate new DC/DC converters with fair low input current ripple, high efficiency, low voltage stress over the power devices, and soft-switching achievement [7-9].

The first offer for this converter is the conventional interleaved parallel boost converter. The main advantage of designing a converter by means of interleaved parallel connected converter is that ripples cancellation in both the input and output waveforms. The dynamic response modification and the magnetic component volume reduction are other features of the interleaving structure [10]. But this topology still has some limitations that prevent using it in the high step up applications. To obtain greater voltage conversion ratio, the interleaved boost converter needs to work in very high duty cycle, which is inefficient and may cause some impairments [11]. The boost converters with coupled inductor are the preeminent solution that ensures high voltage gain while the switch works with low duty ratio [12-14]. Beside the duty cycle, another design factor is provided to enlarge the voltage gain in proportion to the winding turns ratio. Thus, the converter can easily attain high voltage gain; meanwhile the switches tolerate less voltage stress. But, the leakage energy is a destroyer factor in these topologies and causes high-voltage ripples across the switch during its turned-off period. To protect the switch devices and reuse the leakage energy, either a MOSFET with high breakdown voltage and high drain-source resistance $R_{DS(on)}$ or the passive lossless clamp circuit usually adopted [15]. In fact, the passive lossless clamp circuit makes this converter one of indispensable choices in some high voltage applications. But, high voltage stress of the diode, the electromagnetic interference (EMI), and high conduction losses are this topology major weakness. To overcome these drawbacks, an additional resistor–capacitor–diode (RCD) snubber has to be used [16]. The active-clamp circuit is another technique to keep down the switch voltage spike in turn-off duration, which enables soft-switching procedure and reuses the leakage energy [17]. The switching losses are the main factor in the efficiency reduction [18,19]. So, the soft switching should be satisfied in the converters. Some topologies are introduced that attain higher voltage gain by employing the secondary side winding in series with the circuit output stage. In this converter, a suitable turns ratio can be selected to earn a high voltage changeover ratio and low voltage stress over the switches [20]. Several topologies have been derived based on the concept of using the coupled inductors in combination with the voltage doubler rectifier circuit [21, 22]. Merging the coupled inductor with the voltage multiplier cell is a good solution to

wield the leakage energy, degrade the power devices voltage stress, and attain high voltage gain [23, 24]. However the input current with large ripples would hamper their using in the high power cases. One of the best methods to improve the input current ripple issue is the input-parallel coupled inductor based structure that is introduced in [25]. In order to obtain high voltage gain, the secondary and tertiary windings are inserted in series to the output stage of the converter and operate as dc voltage sources that make this converter applicable for high voltage applications with large input current. These multiple windings make the converter bulky and complicate the design procedure and manufacturing.

In this paper, a non-isolated ZVS high step-up dc/dc converter is investigated by employing a switched-capacitor circuit into the conventional interleaved coupled inductor based converter. To share the large input current, attenuate the input current ripple, and degrade the conduction losses, interleaved coupled inductor configuration with asymmetrical pulse with modulation (PWM) control scheme is employed in the input side. Low input current ripple increases the fuel cell stack and the PV module lifetime. To prosper voltage gain ratio, the coupled inductor secondary side winding are connected in series and operate as voltage source in proportion to turn ratio. Also, a voltage rectifier cell composed of switched capacitor cells is embedded in the output side to achieve this target in the relative low value duty cycle. As a result, the voltage stress in the power switches are reduced in proportionate to the turns ratio of the coupled inductors, and the MOSFETs with lower drain-source resistance can be employed, which improves the converter efficiency.

The main merits of the proposed converter are listed as follows: 1) high voltage conversion ratio can be realized by merging two circuits, that is the coupled inductor topology with the switched-capacitor circuit; 2) the coupled inductors transfer the input energy to the load or save in the switched-capacitors during whole switching period; 3) the leakage inductance controls the output diode and the switched-capacitor diodes current, and this is why the reverse-recovery issue is mitigated and the efficiency is increased; 4) Soft switched performance is covered over the whole switching duration and can be fulfilled for both the main and the clamp switches.

After this reviewing section, the operational principle of the proposed converter is presented in section 2 along with its theoretical waveforms. The design parameters are given in section 3. The converter design procedure is illustrated in Section 4 and the experimental waveforms are given in Section 5. The conclusion is given in the final section.

2. THE PROPOSED CONVERTER AND ITS OPERATIONAL PRINCIPLE

The first stage of presented converter is conventional interleaved coupled inductor based converter with active clamp circuit, while the second stage is a voltage rectifier stage composed of switched capacitor cells to provide high voltage conversion ratio. The first stage provides the continuous input current with low ripple and reuses the leakage energies of the coupled inductor. As demonstrated in Fig.1, the coupled inductor model consists of an ideal transformer, the magnetizing inductance, and the leakage inductance.

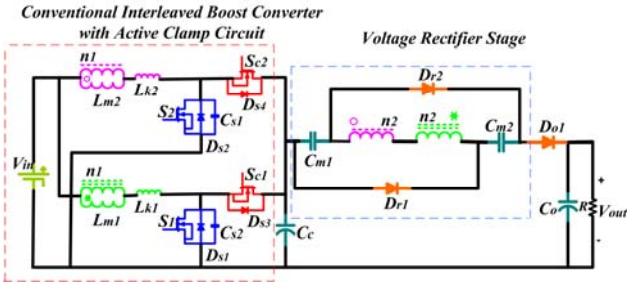

Figure. 1. Proposed non-isolated ZVT boost converter with coupled inductors and switched capacitor.

The parameter N is defined as turn ratio of n_2/n_1. The magnetic coupling method are depicted by "o" and "*", as shown in Fig. 1. The magnetizing inductors are applied paralleled in the input stage as the filter inductors and the secondary windings are inserted in series to the output stage of the circuit and operate as a voltage source to attain high voltage conversion ratio. The left dashed block consists of primary windings of the coupled inductors, the main switches S_1 and S_2, the clamp switches S_{c1} and S_{c2}, and the clamp capacitor C_c. The right dashed block consists of the secondary windings of the coupled inductors, the series capacitor C_{m1} and C_{m2} and two diodes D_{r1} and D_{r2}. Also, D_o is the output diode, V_{in} is the input voltage and V_{out} is the output voltages, and R is the load resistance. The theoretical waveforms of the proposed converter are illustrated in Fig. 2. Sixteen main modes exist in the operation of the investigated converter in the each switching period T_s. Due to symmetrical operation of the interleaved stage, eight modes are studied preciously. The current-flow path corresponding to eight modes is shown.

2.1. Mode 1 [t_0, t_1]

Two switches S_1 and S_2 are turned-on and the voltage rectifier stage diodes D_{r1} and D_{r2} and the output diode D_o are turned off in this time duration. The input current flows through the magnetizing inductors L_{m1} and L_{m2} and the leakage inductances L_{k1} and L_{k2} linearly. The magnetizing inductances L_{m1} and L_{m2} are charged by input voltage V_{in}.

$$i_{m1}(t) = I_{m1}(t_0) - \frac{V_{in}}{L_{m1} + L_{k1}}(t - t_0) \quad (1)$$

$$i_{m2}(t) = I_{m2}(t_0) - \frac{V_{in}}{L_{m2} + L_{k2}}(t - t_0) \quad (2)$$

$$V_{Sc1}(t) = V_{Sc2}(t) = V_{Cc} \quad (3)$$

$$V_{Do}(t) = V_{Dr1}(t) = V_{Dr2}(t) = V_O - V_{Cm} - V_{Cc} \quad (4)$$

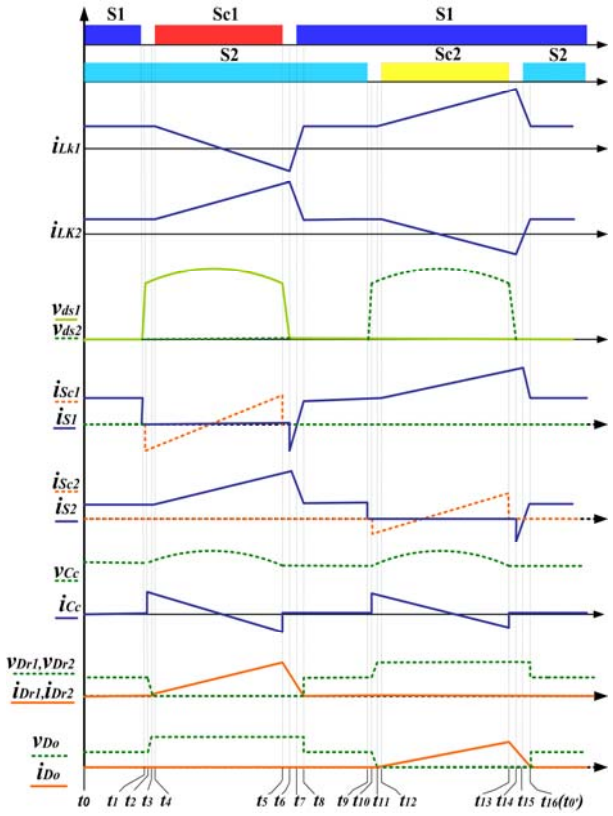

Figure. 2. The theoretical waveforms of the proposed converter.

2.2. Mode 2 [t_1-t_2]

At t_1, the main switch S_1 is ceased to conduct. So, the magnetizing inductance current i_{Lm1} begins to charge the parasitic capacitor C_{s1}. As the parasitic capacitor C_{s1} is very small, all currents flow through it and drain-source voltage of the switch S_1 is rising with constant rate, contemporary. The amount of transferred charge depends on the capacitance of parasitic capacitor and thereby, the parasitic capacitor controls the voltage variation slope. Therefore, zero-voltage-switching operation of the main switch S_1 in the turns-off state is realized.

$$V_{ds1}(t) = \frac{I_{m1}(t_1)V_{in}}{C_{s1}}(t - t_1) \qquad (5)$$

2.3. Mode 3 [t_2-t_3]

At t_2, the drain-source voltage of the clamp switch S_{c1} is fallen to zero and its body diode D_{s2} starts to conduct. At this moment, the current is flowing through the switches in the opposite direction and the voltage of the clamp switch S_{c1} keeps as zero while its gate signal is not applied. This implies the zero-voltage turn-on of the clamp switch S_{c1} is attained. The difference between the input voltage V_{in} and the clamp capacitor voltage V_{Cc} makes the magnetizing inductances L_{m1} to discharge.

2.4. Mode 4 [t_3-t_4]

At t_3, the voltage across the voltage rectifier stage diodes D_{r1} and D_{r2} fall to zero, and then the coupled inductors transmit the input energy to series capacitor C_{m1} and C_{m2}. A resonant circuit is formed composed of the series capacitors C_{m1}, C_{m2}, the clamp capacitor C_c and the leakage inductance of the coupled inductor L_{k1}. Because of considerably large resonant period, the current i_{Lk1} is going up about linearly in this mode. The current through S_2 is summation of the magnetizing inductor current and reflected the secondary winding current. The upper coupled inductor operation is similar to forward converter and the lower one performance is similar to flyback converter.

$$i_{Dr1}(t) = i_{Dr2}(t) = \frac{NV_{Cc} - V_{Cm1}}{2N^2(L_{Lk1} + L_{Lk2})}t \qquad (6)$$

$$i_{Sc1}(t) = i_{Lk1}(t) = i_{Lm1}(t) + 2Ni_{Dr1}(t) = i_{Lm1}(t) + \frac{NV_{Cc} - V_{Cm1}}{N(L_{Lk1} + L_{Lk2})}t \qquad (7)$$

$$i_{S2}(t) = i_{Lk2}(t) = i_{Cc}(t) = i_{Lm2}(t) - 2Ni_{Dr1}(t) = i_{Lm2}(t) - \frac{NV_{Cc} - V_{Cm1}}{N(L_{Lk1} + L_{Lk2})}t \qquad (8)$$

2.5. Mode 5 [t_4-t_5]

At t_4, the gate pulse of the clamp switch S_{c1} is implemented. The operations that will happen in this mode are exactly the same that took place in the fourth mode.

2.6. Mode6 [t_5-t_6]

The clamp switch S_{c1} turns off at t_5 and then the parasitic capacitor energy C_{s1} is delivered to the leakage inductance L_{k1}. A new resonant circuit is created by the switched capacitors C_{m1}, C_{m2}, and L_{Lk1} and C_{s1}. As a result of this resonant circuit, the changing slope of the leakage current is fixed. The voltage increment rate of the switch S_{c1} is confined by C_{s1}; hence zero-voltage-switching operation of the switch S_{c1} is achieved in turn-off interval.

$$V_{ds1}(t) = \frac{I_{m1}(t_5)V_{in}}{C_{s1}}t \qquad (9)$$

2.7. Mode 7 [t_6-t_7]

At t_6, the drain-source voltage of the main switch S_1 goes down to zero and its body diode D_{s1} starts to conduct. The currents descending slope of the voltage rectifier stage diodes D_{r1} and D_{r2} depend on the inductance L_{k1} and L_{k2}.

$$i_{Dr1}(t) = i_{Dr2}(t) = i_{Dr}(t_6) - \frac{V_{Cm1}}{2N^2(L_{Lk1} + L_{Lk2})}t \qquad (10)$$

$$i_{S1}(t) = i_{Lk1}(t) = i_{Lm1}(t) + 2Ni_{Dr1}(t) = i_{Lm1}(t) + 2Ni_{Dr}(t_6) - \frac{V_{Cm1}}{N(L_{Lk1} + L_{Lk2})}t \qquad (11)$$

$$i_{S2}(t) = i_{Lk2}(t) = i_{Lm2}(t) - 2Ni_{Dr1}(t) = i_{Lm2}(t) - 2Ni_{Dr}(t_6) + \frac{V_{Cm1}}{N(L_{Lk1} + L_{Lk2})}t \qquad (12)$$

2.8. Mode 8 [t_7-t_8]

At t_7, the gate pulse of the main switch S_1 is applied. As the current is passing through the switch before its gate pulse comes, the zero-voltage turn-on performance is reached. The currents through the voltage rectifier stage D_{r1} and D_{r2} fall to zero at t_8, and then, the voltage rectifier stage diodes are stopped to conduct. The magnetizing inductance L_{m1} and the

leakage inductance L_{k1} are charged by the input voltage in this interval.

The rest switching sequence starts at t_8 and is similar to first half cycle except with commutation processes happen between S_2 and S_{c2} and the current goes through output diode D_o in the voltage rectifier stage. Following this fact, the series capacitor C_{m1} and C_{m2} are discharged and the energy is transferred to the output capacitor C_o. The current flow-path in the voltage rectifier stage in the whole switching period is demonstrated in Fig.3.

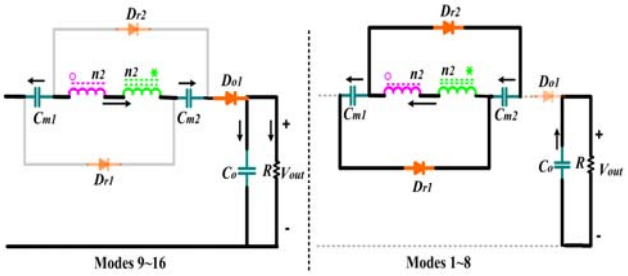

Figure. 3. The current flow-path in the voltage rectifier stage in the whole switching period.

3. CONVERTER STEADY STATE OPERATION ANALYSIS

To obtain converter design parameters some assumption are assumed as the voltage of the output capacitor, the clamp capacitor, and two switched capacitors C_{m1} and C_{m2} are considered constant during the whole switching period. Also, the parameters of the two coupled inductors are supposed the same. In addition, two modes depended on the dead time between the switches gate pulses are ignored.

$$L_{m1}=L_{m2}=L_m \quad (13)$$

$$L_{k1}=L_{k2}=L_k \quad (14)$$

$$C_{m1}=C_{m2}=C_m \quad (15)$$

3.1. Voltage Conversion Ratio

Since the average voltage of the magnetizing inductor must be zero during the whole switching period in the steady-state, the voltage of the clamp capacitor can be expressed by

$$V_{Cc}=\frac{V_{in}}{1-D} \quad (16)$$

Because of the voltage-second balance on the secondary winding of the coupled inductors, the voltage of the rectifier stage capacitors C_{m1} and C_{m2} can be obtained by

$$Vc_{m1}=Vc_{m2}=\frac{V_{out}-V_{Cc}}{3} \quad (17)$$

Due to utilizing large clamp capacitor to limit the voltage surge on the switches, the resonant period of the circuit composed of the clamp capacitor and the leakage inductance is very larger than the switching period. Similar to mode 3, the leakage inductance current and the output diode current vary linearly. As mentioned in the previous section and from Fig .4, the current rising slope of the voltage rectifier stage diodes D_{r1} and D_{r2} and their maximum value in the mode 4 can be derived as follow.

$$k_{rise}=\frac{NV_{Cc}-V_{Cm}}{4.N^2.L_k} \quad (18)$$

$$I_{Dr1-peak}=I_{Dr2-peak}=K_{rise}.(1-D)T_s \quad (19)$$

The current descending slope of the voltage rectifier stage diodes D_{r1} and D_{r2} is controlled by leakage inductance L_k in the turn-off interval, mode 6.This slope can be written as follows:

$$k_{fall}=-\frac{V_{Cm}}{4.N^2.L_k} \quad (20)$$

Therefore, the fall time of the rectifier stage diodes current can be derived by

$$t_{fall}=-\frac{I_{Dr1-peak}}{K_{fall}}=\frac{NV_{Cc}-V_{Cm}}{V_{Cm}}(1-D)T_s \quad (21)$$

Since the average current of the switched capacitors C_{m1} and C_{m2} must be zero, the average output current I_o is expressed by

$$I_o=\frac{V_{out}}{R}=\frac{1}{2}I_{Dr1-peak}[(1-D)T_s+t_{fall}].f_s \quad (22)$$

From (16)-(22), the voltage conversion ratio of the converter can be calculated by

$$M=\frac{V_{out}}{V_{in}}=\frac{2(3N+1)}{(1-D)-\frac{4Nk_M(3N+1)}{(N+1)(1-D)}+\Delta} \quad (23)$$

where $k_M=(L_k.f_s)/R$ and

$$\Delta=\sqrt{[(1-D)-\frac{4Nk_M(3N+1)}{(1-D)(N+1)}]^2+16Nk_M(3N+1)}$$

The dependency of the voltage conversion with the duty-cycle in different leakage inductances is sketched in Fig. 5(a). This fact can be revealed that at a certain condition, as the leakage inductance enhances, the voltage conversion ratio detracts. The relationship between the voltage gain and the duty-cycle under various turn ratios is shown in Fig.5 (b). It can be concluded that another design parameter is provided for designer to achieve high voltage gain by turns ratio of the coupled inductor

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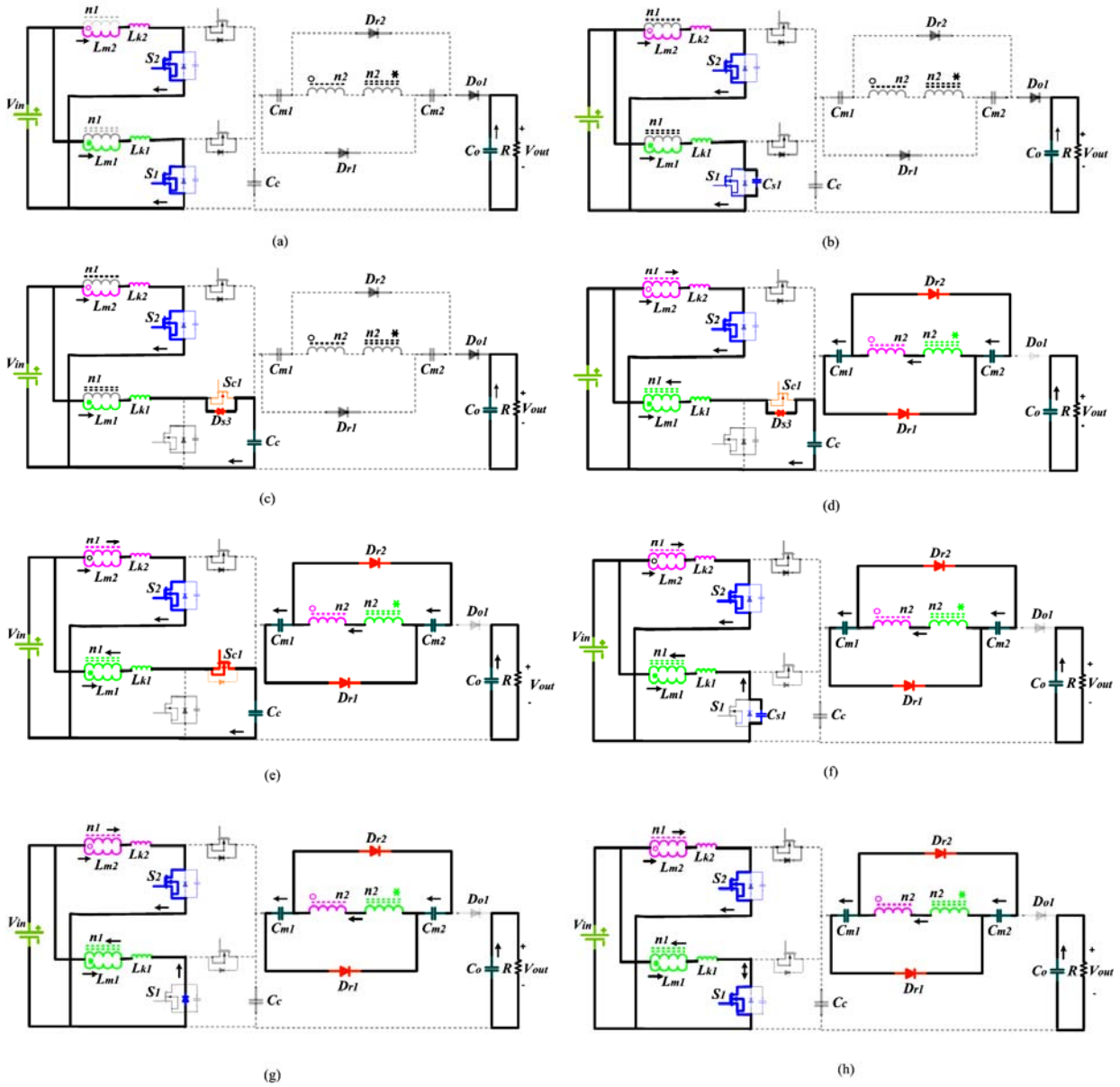

Figure. 4. Operation processes of proposed converter: (a) Stage 1 [t_0-t_1]; (b) Stage 2 [t_1-t_2]; (c) Stage 3 [t_2-t_3]; (d) Stage 4 [t_3-t_4]; (e) Stage 5 [t_4-t_5]; (f) Stage 6 [t_5-t_6]; (g) Stage 7 [t_6-t_7]; (h) Stage 8 [t_7-t_8]

3.2. Voltage Stresses of the Power Switches and Output Diodes

The main switches and the clamp switches are subjected to the voltage across the clamp capacitor C_c, which is given by

$$V_{stress-main} = V_{stress-clamp} = \frac{V_{in}}{1-D} \approx \frac{V_{out}}{3N+1} \quad (24)$$

The voltage stress of the diode D_{r1}, D_{r2} and D_o can be derived by

$$V_{stress-D_{r1}} = V_{stress-D_{r2}} = V_{stress-D_o} = V_{out} - V_{Cc} - V_{Cm} = \frac{2N}{3N+1} V_{out} \quad (25)$$

The diagram of the normalized diodes and switches voltage stress with the turns ratio of the coupled inductors is demonstrated in Fig. 6. An important fact is shown in this figure that the voltage stress of the semiconductor elements is a function of the turns ratio of the coupled inductors. Thus a right turns ratio should be chosen to confine the drain-source voltage of the switches. Thereby, the efficiency of the presented converter can be improved by employing switches with low $R_{ds(on)}$. It can be observed that all diodes experience voltage stress lower than the output voltage. So, the diodes with lower inverse-recovery time can be utilized to enrich the efficiency.

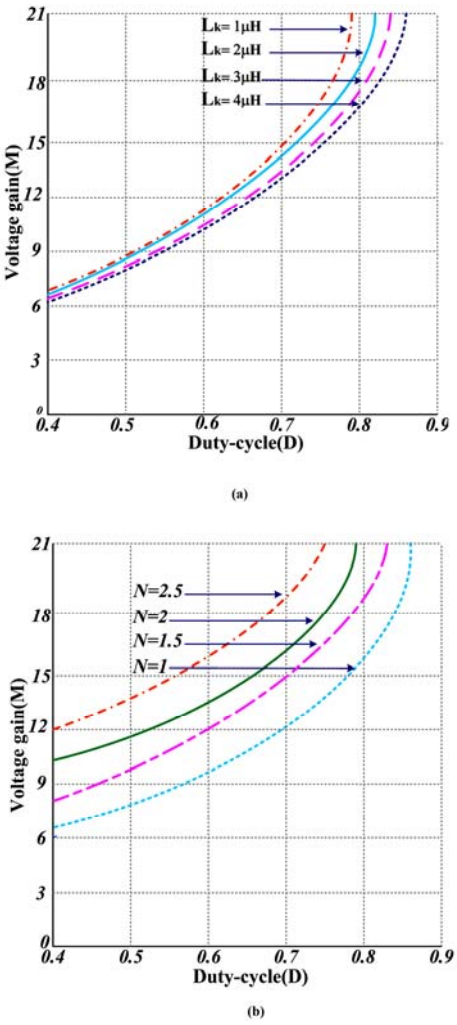

Figure. 5. Voltage gain of proposed converter: (a) voltage gain with different leakage inductances; (b) voltage gain with different turns ratio.

3.3. Soft Switching Qualification

The ZVS turn-on operation is another great feature of the investigated converter. As illustrated in section II, the turn on soft switching is attained in mode 3 and 8 for switches S_{c1} and S_1, respectively. This performance is guaranteed if the energy stored in the leakage inductance at t_7 be larger than the energy stored in the parasitic capacitor C_{s1}. The ZVS qualification of the main switches is expressed by

$$\left|\frac{1}{2}L_k\, i_{Lk}^2(t) \ge \frac{1}{2}C_S\left(\frac{V_{in}}{1-D}\right)^2\right| t = t_7 \text{ or } t = t_{15} \qquad (26)$$

Where,

$$i_{Lk}(t_7) = \frac{I_{in}}{2} - \frac{4NI_{out}}{1-D} \quad \text{and}$$

$$i_{Lk}(t_{15}) = \frac{I_{in}}{2} - \frac{2NI_{out}}{1-D}$$

Also, the ZVS turn-on of the clamp switches is ever realized because their ant parallel diodes are in the on state before the turn on signals are applied to the gates. From (26), a boundary switch current between ZVS region and hard switching region can be derived as follows:

$$I_{o,ZVS-S_1} = \sqrt{\frac{C_s}{L_k}}\,\frac{V_{out}}{\left(\frac{M}{2} - \frac{4N}{1-D}\right)(3N+1)} \qquad (27)$$

$$I_{o,ZVS-S_2} = \sqrt{\frac{C_s}{L_k}}\,\frac{V_{out}}{\left(\frac{M}{2} - \frac{2N}{1-D}\right)(3N+1)} \qquad (28)$$

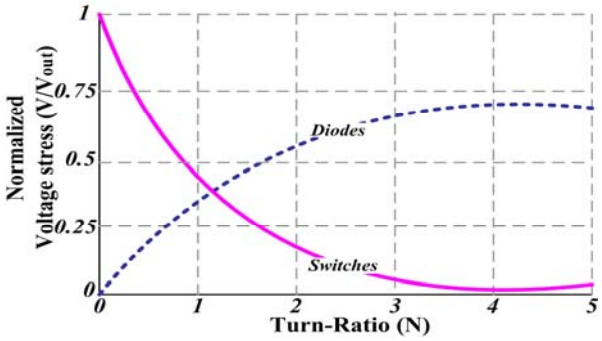

Figure. 6. Relationship between normalized diodes and switches voltage stress with turns ratio.

The relationship between the load current and the leakage inductance concern to implement the ZVS soft switching performance for two main switches S_1 and S_2 is sketched in Fig.7.

The descending slope of the output diode and the voltage rectifier cell diodes are moderated by the leakage inductance of the coupled inductor L_k, which alleviates the reverse-recovery issue and meliorate the converter efficiency. From (10), the turn-off descending slope in mode 7 and 15 is given by

$$\frac{di_{Do}(t)}{dt} = \frac{di_{Dr1}(t)}{dt} = \frac{di_{Dr2}(t)}{dt} = \frac{V_{out}}{N(3N+1)L_{Lk}} \qquad (29)$$

From the aforementioned equation, a large leakage inductance is needed to mitigate the reverse-recovery current, while as sketched in Fig.3, in order to obtain higher voltage gain in constant load, the smaller leakage inductance are required. So a compromise must be done in the leakage inductance selection.

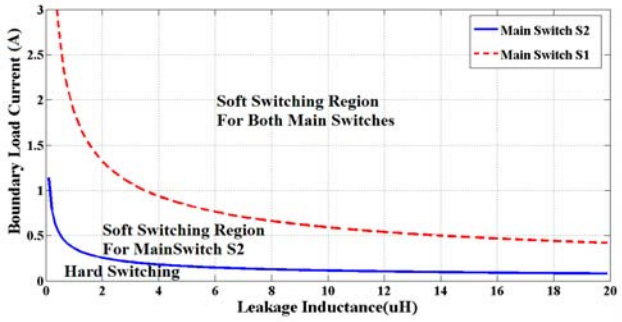

Figure. 7. Soft switching operation.

4. DESIGN PROCEDURE

4.1. Turn ratio

The turns ratio is an effective parameter in the circuit design, because it provides a control variable to choose the semiconductor devices. It can be determined from the ideal voltage gain relation by setting the maximum duty cycle as 0.7.

$$N = \frac{V_{out}(1-D_{\max})}{3V_{in}} - \frac{1}{3} \tag{30}$$

4.2. Magnetizing inductance

In order to decrease the input current to the standard value, the magnetizing inductor can be selected from (1), which is given by

$$L_m \geq \frac{D T_S V_{in}}{\Delta I_m} \tag{31}$$

4.3. Leakage inductance

The maximum leakage inductance to achieve real voltage gain can be concluded from (23) and the minimum leakage inductance guarantee the soft switching performance can be determined from (26) as follow:

$$L_{Lk,\min} \geq \frac{(\frac{M}{2} - \frac{4N}{1-D})^2 . C_S . R_{out}^2}{(3N+1)^2} \tag{32}$$

4.4. Selection of Power devices

As mentioned in the steady-state operation section, the voltage stresses of the power switches are equal with the clamp capacitor voltage, which is given by

$$V_{stress-main} = V_{stress-clamp} = \frac{V_{in}}{1-D} \approx \frac{V_{out}}{3N+1} \tag{33}$$

The root-mean-square current of the main switch S_1 is given by

$$I_{RMS-S1} = \frac{I_{out}}{(1-D)} \sqrt{\frac{(52+27D)N^2 + (12+18D)N + 3D}{12}} \tag{34}$$

The root-mean-square current of the main switch S_2 is given by

$$I_{RMS-S2} = \frac{I_{out}}{(1-D)} \sqrt{\frac{(136-109D)N^2 + (24-6D)N + 3D}{12}} \tag{35}$$

The root-mean-square currents of the clamp switches are given by

$$I_{RMS-Sc1} = I_{RMS-Sc2} = \frac{(3N+1)I_{out}}{2\sqrt{3(1-D)}} \tag{36}$$

Also, the voltage stresses of the diodes are derived from (4) as follow:

$$V_{stress-D_{r1}} = V_{stress-D_{r2}} = V_{stress-D_o} = \frac{2N}{3N+1} V_{out} \tag{37}$$

The peak value of the diodes current is

$$I_{peak-D_{r1}} = I_{peak-D_{r2}} = I_{peak-D_o} = \frac{2I_{out}}{1-D} \tag{38}$$

4.5. Selection of clamp capacitor

The active clamp circuit is utilized to confine the voltage surge on the switches; therefore the clamp capacitor value should be high. A standard for the clamp capacitor choosing is that one-half of the resonant period outlast than the turn-off duration of the main switches to avoid resonant ringing, which is given by

$$C_c \geq \frac{(1-D)^2 T_S^2}{2\pi^2 L_k} \tag{39}$$

4.6. Selection of parallel capacitor C_{s1} and C_{s2}

To achieve zero voltage switching operation in the switches turn-off state, the parallel capacitors C_{s1} and C_{s2} can be designed from (5).

4.7. Selection of switched capacitor C_{m1} and C_{m2}

In the steady-state analysis assumed that the switched capacitor act as dc voltage sources, therefore the voltage ripple of these capacitors should be in the standard range. From Fig. 4, both the average current of the capacitors C_{m1} and C_{m2} in the charging state and discharging state are equal to the load current. So, the capacitances of C_{m1} and C_{m2} can be calculated by

$$C_{m1} = C_{m2} \geq \frac{T_S V_{out}}{R . \Delta V_{out}} \tag{40}$$

5. EXPERIMENTAL RESULTS

In order to demonstrate the effectiveness of the theoretical analysis, a 1-kW laboratory prototype is established and its parameters are given in table 1. Fig.8 (a) to Fig.8 (e) shows the waveform of the proposed converter at full load state with 30V input voltage. The input current i_{in} and the leakage inductances current i_{Lk1} and i_{Lk2} are displayed in Fig. 8 (a). It can be observed that the input current ripple is very low and a small capacitor can be employed as input filter, so improve the performance and lifetime of the PV and FC systems. Fig.8 (b) illustrates and current and the drain- source voltage waveforms of the main switch S_1. This fact can be revealed from waveforms that the ZVS operation of the main switch in turn-on state is attained. Because the drain-source voltage becomes zero firstly and afterward, the main switch current flow in opposite direction. The waveforms of the clamp circuit current and voltage and the gate-source voltage of the clamp switch S_{c2} are given in Fig.8 (c). It is obvious that the leakage inductances current flows through the clamp circuit in turn-off that interval of the main switches and the drain-source voltage of the switch s_{c2} is confined effectively to that of the capacitor C_c. The experimental waveforms of the voltage V_{cm1} and the current i_{cm1} on the switched capacitor C_{m1} is shown in Fig.8 (d). The low ripples across capacitor voltage V_{cm1} support the switched capacitor design procedure. The current and voltage waveforms of the voltage Rectifier stage diode D_{r1} and the output diode D_o are

depicted in Fig.8 (e). It can be observed that the voltage stresses of the diodes are almost 190V and the diodes current in reversed-biased state is detracted to zero proximately, hence the inverse-recovery problem is lightened. Fig .9 indicates the efficiency comparison with the investigated topology and the conventional interleaved converter at various loads with different input voltages. The highest efficiency of the proposed converter is 95.9% with 40V input voltage. It can be seen that almost 8% efficiency development in the full load condition is achieved over the conventional
interleaved converter.

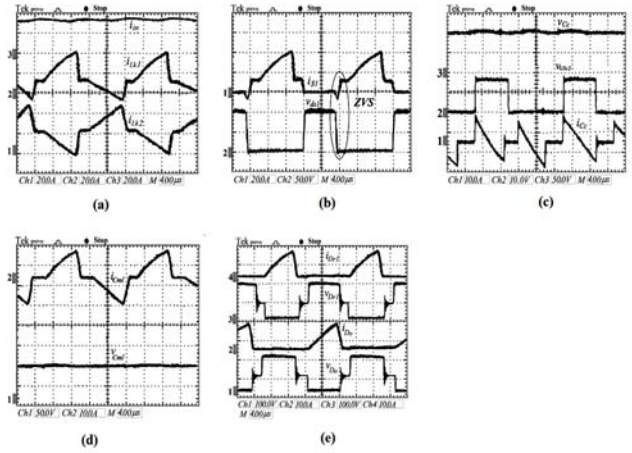

Figure. 8. Fig.8 (a) to Fig.8 (e) show the waveform of the proposed converter at full load state with 30V input voltage.

6. CONCLUSION

A non-isolated interleaved converter with coupled inductor circuit is proposed for high step-up application. By merging a voltage rectifier stage with the interleaved coupled inductor based converter, a new configuration with high voltage conversion ratio is derived. Employing the input-parallel structure makes this converter appropriate for high current applications, because the input current is divided between two paths. In order to confine the switches voltage in turn-off interval and accomplish the ZVS soft-switched operation, the active clamp scheme is exerted. Also, the leakage inductances of the coupled inductors are used to achieve ZCS performance of the diodes, regulate the diode current descending rate, and attenuate the reverse-recovery current. The analysis showed that there is a trade-off between the voltage gain and ZVS implementation. The design criterion is to decrease the leakage inductance as low as possible while keeping the zero voltage switching operation. Finally, a 1kW prototype converter is implemented to confirm the theoretical analysis.

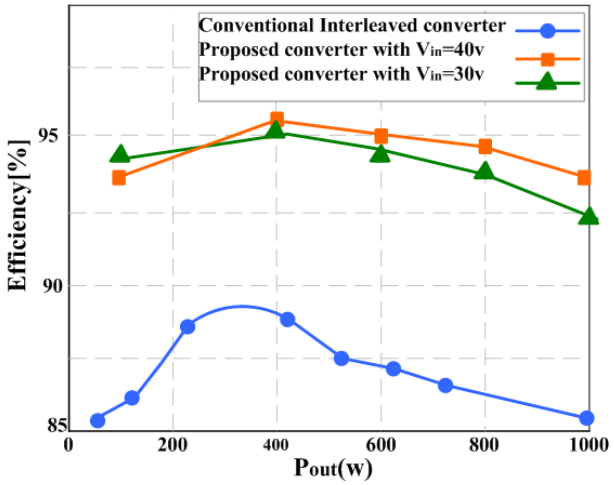

Figure. 9. The efficiency comparison with the investigated topology and the conventional interleaved converter at various loads with different input voltages.

TABLE 1.
PARAMETERS OF IMPLEMENTED CONVERTER.

Part	Value
Input Voltage V_{in}	30-45 V
Output Voltage V_o	380 V
Output Power P_o	1000 W
Switching frequency f_s	50 kHz
Turns ratio $(N=n_2/n_1)$	25/20
Main Switches (S_1 and S_2)	IRFP4227
Clamp Switches (S_{c1} and S_{c2})	IRFP4227
Voltage rectifier stage diodes (D_{r1}, D_{r2}) and Output diode (D_o)	MUR1540
Clamp capacitor C_c	4.7µF
Voltage rectifier Stage Capacitors(C_{m1} and C_{m2})	4.7µF
Output Capacitor (C_o)	470µF
Parallel Capacitor (C_{s1} and C_{s2})	2.2nF
Magnetizing Inductors	200µH
Leakage Inductances(L_{k1} and L_{k2})	3µH

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