SURVEY OF NETWORK ON CHIP ARCHITECTURES

Muhammad Athar Javed Sethi, Fawnizu Azmadi Hussin, Nor Hisham Hamid

Department of Electrical & Electronic Engineering, Universiti Teknologi PETRONAS, Tronoh, Perak, Malaysia.

Corresponding Author: atharsethi@yahoo.com

ABSTRACT: Network on Chip (NoC) is a communication paradigm for on-chip communication. It has replaced the traditional bus and crossbar interconnection as it has higher bandwidth, modularity, scalability and benefits of resource reuse. This paper presents the detail survey of the NoC architectures being proposed and implemented in last more than a decade. Apart from comparing the NoC architectures on different parameters, detail information is also provided about these parameters of NoC architecture.

Key words: *Network on Chip (NoC); Routing algorithms; Switching techniques; Clocking mechanism*

1. INTRODUCTION

Network on chip (NoC) is a communication framework for multicores connected together in regular or irregular topologies. The various topologies of NoC can be mesh, torus, tree, ring, or it can be a hybrid topology. NoC is constructed from routers, processing elements (PE's), network interface (NI) and interconnects (links). Routers are connected together through interconnects. PE's are connected to routers through NI's. NI separate the data communication of PE's from inter router communication. NI transforms the message generated by PE's to the packet format which router understands. Routers send these packets to the neighbor routers so that it can reach at the destination. PE's can be homogeneous devices or it can be heterogeneous devices. The PE's can be a cache, reconfigurable devices, memory, or any other processing element [1].

Network on chip have replaced the traditional bus based wiring between PE's with a network. In NoC resources are well structured and arranged in a particular topology. This makes the NoC scalable and modular. NoC have higher bandwidth as compared to bus and they support multiple parallel communications. NoC is more organized, it provides efficient utilization of the network resources and have better cost and performance parameters as compared to global wires between PE's [2].

An on chip interconnection network SPIN[3] was proposed in 2000. This put a research foundation for on chip communication algorithm and architectures. Later in 2001, Dally [2] further refined the on chip interconnection network and proposed folded torus based on-chip architecture. The router architect is also explained in this paper. Later, in 2002, Luca Benini named this on chip interconnection network as Network on Chip (NoC) [4]. In this survey paper, various NoC architectures have been reviewed based on the different parameters [1-3, 5-113].

2. Motivation

The purpose of this survey study is to review the existing NoC architectures from different perspectives (parameters). Most of the papers in the literature only review few architectures in their paper and the explanation is specific to their application or domain of the paper. In order to fill the gap and help the research community this survey study is conducted in which more than 100 different NoC architectures are reviewed. This study will help the individuals and researchers about the different characteristics behavior of the NoC architectures. This will help them to find the important and un-resolved issues for further investigation, research and further contribute to the NoC field. To the best of our knowledge, this is the most comprehensive literature review of NoC architectures.

There are few other survey studies on NoC architectures [114-117] but they cover the basic trends, principles and working mechanism of network on chip. These survey studies are not covering the broader spectrum of NoC architectures using various parameters. The survey study [114] is very well written but explains the general trends in NoC research and practices. This survey study only covers eight NoC architectures based on few parameters. The survey study [115] covers sixty eight NoC architectures. The comparison is more qualitative then quantitative. The survey study was published in 2008 and it not up to date. The survey study [116] was published in 2012 and it covers seventy seven different NoC architectures. These architectures are compared based on only four parameters. The parameters include year, switching, topologies and implementation. The survey paper [117] is only covering four NoC architectures using qualitative description. This paper explains the basic principles of NoC which include routing algorithm, switching, flow control techniques and other mechanisms.

The NoC has brought the tremendous change in the on-chip communication mechanism. It has replaced the traditional wires with the routers and interconnects. The bus between multiple components was not able to cope with communication requirements of them. Scientists come up with the idea of multiprocessors system on chip (MPSoC). This improved the performance of the embedded systems but later, the bus between multi components of embedded systems were not able to cope the heterogeneous and challenging communication requirements of MPSoCs. This leads to the idea of Network on Chip (NoC) by researchers and scientists. The NoC have adapted a lot of difficult and complex concepts of data communication to address the communication requirements between MPSoC [118].

The current literature on the NoC lacks the in depth details of concepts related to this area. This paper is focusing on the parameters which are used by the NoC architectures. The parameters on which the survey study is based on are Link sharing mechanism, Routing algorithm, Connection types, Quality of service (QoS) and Switching techniques.

We believe that the detail information of the parameters along

with the real NoC architecture examples will help the research community to know about the current trends in the NoC. This survey paper is also highlighting and gathering the key aspects of NoC from various sources which will act as catalyst for further research.

1. Link Sharing Mechanism:

Link sharing mechanism defined the way how communication channel is shared between multiple sources and destination in NoC. Link sharing mechanisms are basically divided into two broad categories, circuit switching and packet switching (connection oriented and connection less). According to survey study most of the NoC architectures are using packet switching while only few are using circuit switching. Two architectures are using SDM based packet switching technique and other is using WDM for link sharing. This clearly shows the scientists are more interested in effective and efficient utilization of resources as compared to allocating the resources for particular time period. In circuit switching based connections the resources can be underutilized at certain times.

The circuit switching connections also lacks the reactivity to certain rapid changes in the bandwidth and throughput requirements by PE's [3]. In order to efficiently utilize the bandwidth of the NoC, the concept of virtual channels were introduced using time division multiplexing [14], frequency division multiplexing or combination of both these techniques [101]. Despite of these drawbacks of circuit switching technique it is still being used by NoC applications which required guaranteed services [119]. The future link sharing mechanism should include adaptive and hybridize mechanism which can switch between circuit and packet switching based on the traffic load and PE requirement.

1.1 Circuit Switching

In circuit switching a physical link is established between source and destination before data transmission. After the connection establishment flits (flow control digits) or packets traverses the various routers. The connection is established until the all packets are received at the destination [120]. The circuit switching technique is better for high traffic real time applications. These applications generated and send traffic at a higher injection rate. As there is a separate link between source and destination that's why there is no delay communication problem and high throughput can be achieved. In circuit switching technique bandwidth is reserved for entire duration of data but resources (routers, links) are busy until complete data is received at the destination. The setup of path from source to destination increases unnecessary delay [121]. Dally et al.[2], SoCBUS[13], OCN[16], Nexus[21], Wolkotte et. al. [41], PNoC[56], Cross road interconnection architecture[62], Ambric[73], EIB on chip network[75], CSRA-NoC[80] and Ramos et. al.[98] are architectures which are based on circuit switching techniques. Dally et. al. NoC architecture provides virtual channel based circuit switching while OCN provides circuit switching using round robin arbitration. The only drawbacks of the techniques adopting circuit switching are the average utilization of the link. The links are underutilized at certain instant of the time. Therefore, in order to address these issues packet switching must also be used in these systems in order to efficiently utilize the communication channel [12].

1.2 Packet Switching

In packet switching, messages are divided in to packets and flits. The router propagates the flit in a particular direction based on the routing algorithm [122]. Routing algorithm can be deterministic, stochastic, full adaptive and partial adaptive. These routing algorithms are explained in section 2. There are number of architectures which are based on packet switching. They are CLICHÉ[1], SPIN[3], aSOC[5], MicroNetwork[6], PROTEO[8], CHAIN[9], RAW[10], Eclipse[11], HERMES[14], SoCIN[17], Nostrum[19, 20], Xpipes[22], R2NoC[23], Spidergon[27], RaSoC[28], QNoC[29], NoCGen[31], Reconfigurable Network on Chip[32], DyAD[33], Asynchronous On chip network router with Quality of Service[35], Black-Bus[36], SNA[37], Topology adaptive NoC[43], Arteris[45], DyNoC[46], Asynchronous NoC Architecture[48], DSPIN[52], INoC[53], XGFT[54], CTNOC[57], Low latency on chip network[58], GEXPolygon & GEXSpidergon[59], CoNoChi[61], Communication Architecture Optimization[66], TILEPro64[70], STNoC[74], SCC[76], MoCRes[77], Generalized de Bruijn Graph NoC[78], Polaris[79], artNoC[81], CDMA NoC[82], A reconfigurable baseband platform based on Asynchronous NoC[83], EVC[85], Aelite[88], XHiNoC[90], Network on Chip in a Three Dimensional[91], BiNoC[92], ALPIN[93], DRNoC[95], PMCNOC[96], Dynamic Reconfigurable Network on Chip[97], WiNoC[101], dAElite[102], BMNoC[103], Custom Network on Chip Architecture[104], DANoC[105], WaveSync[106], AdNoC[107], Mesh based NoC[109] and BLOCON[112].

1.2.1 Spatial and Wavelength division multiplexing (SDM & WDM)

Spatial division and wave length division multiplexing are link sharing techniques being used by some of the NoC architectures. SDM physically divides every link and buffer into multiple virtual circuits. Every virtual circuit is assigned the portion of the bandwidth. SDM uses the wormhole switching for flow control [123]. An Architecture and compiler for aSoC[24] and Spatial Division Multiplexing NoC[44] are two example of spatial division multiplexing. WDM can send multiple signals simultaneously to attain higher throughput. The wavelength determines the destination address in wavelength division multiplexing or routing. This makes the WDM as contention free link sharing mechanism. ORNoC[99], NoC architectures is providing link sharing using WDM. Some of the architectures have not provided any information regarding their link sharing mechanism.

2. Routing Algorithms:

Routing algorithm defines the path for the packet between source PE and destination PE. There are basically four broad categories of routing algorithms. They are deterministic, stochastic, fully adaptive and partial adaptive routing algorithms. When the routing decision is taken by source it is called source routing while when the immediate nodes of the NoC take the decision then routing algorithm is categorize as distributed routing [14]. The trends of using routing algorithms are that 43% NoC architectures have used deterministic routing algorithm while 19% architectures are using fully adaptive routing algorithms. While none of the

NoC architectures have used the stochastic routing algorithm. Deterministic routing algorithms require fewer resources as compared to adaptive routing algorithm. These algorithms deliver an orderly packet as compared to adaptive routing algorithm. Adaptive routing algorithms provide better throughput and low latency by having alternate paths due to congested or faulty paths. Deterministic and partially adaptive algorithms are deadlock and livelock free while fully adaptive algorithms requires some precaution by having deadlock, livelock and congestion avoiding techniques [119]. Adaptive routing algorithms need special modules at the receiver to reorder the packets, which in turns increases the design complexity and latency of the packets. Deterministic routing algorithms perform well under uniform traffic pattern while adaptive routing algorithms are preferred for bursty and irregular traffic [124]. Few NoC architectures have not specified or it's not clear which routing algorithm they are using. Scientists have chosen the deterministic routing algorithms because of simplicity as they are less complex to implement.

2.1 Deterministic Routing Algorithms

In deterministic routing the packet routes from the certain point to another using a fixed path. These algorithms lack the adaptiveness. Xy, yx, xyz and zyx [125-131] are few examples of dimension order routing (DOR) algorithms. DOR algorithms are the simplest algorithm of deterministic routing algorithms. These DOR algorithms are deadlock free. In minimal path routing, the packet can traverse using multiple (shortest) paths to reach at the destination. Minimal path routing algorithms are prone to deadlock as compared to DOR [132].

Most of the NoC architectures are based on static and deterministic routing. The NoC architectures are; CLICHÉ[1], Dally et al. [2], aSOC[5], OCTAGON[7], Eclipse[11], HERMES[14], OCN[16], SoCIN[17], Nexus[21], Xpipes[22], µSpider[25], Spidergon[27], RaSoC[28], QNoC[29], DyAD[33], A routing switch for on chip interconnection networks[34], Asynchronous On chip network router with Quality of Service[35], Mango[38-40], Topology adaptive NoC[43], Spatial Division Multiplexing NoC[44], DyNoC[46], Asynchronous NoC Architecture[48], DSPIN[52], XGFT[54], PNoC[56], CTNOC[57], CoNoChi[61], Cross road interconnection architecture[62], HIBI[63], ProtoNoC[67], TILEPro64[70], UT TRIPS[71], SCC[76], MoCRes[77], Polaris[79], artNoC[81], EVC[85], MoCSYS[87], XHiNoC[90], BiNoC[92], DRNoC[95], PMCNOC[96], Ramos et. al. [98], DANoC[105], AdNoC[107], Mesh based NoC[109] and HELIX[113].

2.2 Stochastic Routing Algorithms

Packets are broadcasted in all or particular direction depending on the type of stochastic routing algorithm. The benefits of these algorithms are that they are easy to implement and they are not complex. But the drawbacks of these techniques are that they are not dynamic in nature as the replicate the packets in all direction. They consume high energy and bandwidth. They have deadlock and livelocks problems. These algorithms do not perform well even at low traffic rate. Stochastic routing algorithms provide fault tolerance, adaptability through data redundancy and by eating up the bandwidth of the NoC. Probabilistic gossip flooding scheme, directed flooding, N-Random walk, source routing [125, 126, 133] and connection oriented stochastic routing (COSR) [133] are few examples of stochastic routing algorithm.

2.3 Fully adaptive Routing Algorithms

The routing at fully adaptive algorithms depends upon the routing table or on the routing information collected from the neighbor nodes at router. Based on this information the direction of the packet is decided at run time. Routers constantly communicate with each other to update the routing table or neighbor nodes information. Updating of routing information takes a lot power, energy and time, which affects the throughput of the NoC [125, 134]. Source routing for NoC (SRN) and force directed wormhole routing (FDWR) are two examples of fully adaptive routing algorithm [127, 128]. Fully adaptive routing algorithms are very dynamic but updating of routing information consumes a lot of area, energy and power which sometimes degrade the performance of NoC. The flow of control messages between routers at times creates congestion, deadlock situation in NoC. The techniques [135, 136] are fully adaptive routing algorithm but they does not have the routing table. They collect the neighbor information through certain control messages. Based on this information, router makes a decision in which direction the packet should be routed.

CHAIN[9], Æthereal[12], BIDI-MIN[15], Mango[38-40], Kavaldjiev et. al.[51], Intel TeraFLOPS[72], Generalized de Bruijn Graph NoC[78], TTNoC[84], Aelite[88] and HT-OCTAGON[89] are few NoC architectures which uses source based routing. While SPIN[3], PROTEO[8], A 0.13µm NoC[26], Adaptive Network on Chip[49], A low latency router[50], XGFT[54], High Throughput NoC Architecture[55], GEXPolygon & GEXSpidergon[59], Dynamic reconfigurable NoC for adaptive reconfigurable MPSoC[65], Polaris[79] and DRNoC[95] supports adaptive routing algorithms.

2.4 Partial adaptive Routing Algorithms

Partial adaptive algorithms as the names suggests are partially adaptive. They put some restrictions on the routes which can be taken by router in NoC [14]. These algorithms solve the problem of deadlock and also consume less energy and power as there are no routing tables in it. These algorithms limit the adaptiveness of the NoC and latency of the packets increases due to restrictions [125]. West first, negative first, north last, south last, odd-even and planar adaptive [125, 126, 129-131, 134, 137, 138] are few examples of these algorithms.

artNoC[81], XHiNoC[90], Dynamic Reconfigurable Network on Chip[97], WaveSync[106], Mesh based NoC[109] and SWIFT[111] have turn based adaptive routing algorithms. While RAW[10], µSpider[25], NoCGen[31], DyAD[33], Asynchronous NoC Architecture[48], SCC[76], A reconfigurable baseband platform based on Asynchronous NoC[83], XHiNoC[90], BiNoC[92] and Mesh based NoC[109] have odd-even routing algorithms.

2.5 Bio-inspired routing algorithms

Bio-inspired NoC algorithms are a novel way to address the limitations of these traditional NoC algorithms. The idea of bio-inspired algorithms is to take inspiration from the nature

to solve the complex and difficult engineering world problems [139]. The bio-inspired algorithm [140] is autonomic by implementing and getting inspiration from the self-configuration, self-healing and self-optimization characteristics of biological immune systems. Two techniques [135, 136, 141] are being inspired by the biological brain robustness and fault tolerance. These techniques have implemented and adopted the self-adapt, self-heal concept of the biological brain in NoC. These bio-inspired techniques have implemented the biological techniques "synaptogenesis" and "sprouting" in NoC to make it fault tolerant and robust.

SoCBUS[13], R2NoC[23], Wolkotte et. al.[41], TTNoC[68], WiNoC [101] and dAElite[102] are few NoC architecture which have distributed routing algorithm. While Nostrum[19, 20] have TDM based deflective routing algorithm. Other NoC architectures are following stream based routing, e-cube routing, Dijsktra shortest path routing, shortest distance, shortest path first and temperature first routing algorithms.

3. Connection Types:

A connection type refers the way source PE is connected with the destination PE. There can be simple or unicast (1-1), narrowcast and multicast connections. Most of the NoC architectures are supporting simple connections by 36% while multicast and broadcast communication types are used by 17% and 3% NoC architectures. Three NoC architectures support broadcast communication while only one architecture supports multipath routing.

The multicast communication produces significant amount of redundant traffic which increases the latency and congestion in NoC as compared to unicast communication. By combining multiple unicast connections, multicast communication can be constructed to overcome the drawbacks of multicast communication. Various MPSoC applications use multicast communication which includes replication, barrier synchronization, cache coherency in distributed shared memory architecture [124].

3.1 Simple connection

1-1, simple or unicast connection is between one source PE and a destination PE [142]. SPIN[3], aSOC[5], OCTAGON[7], CHAIN[9], Æthereal[12], SoCBUS[13], HERMES[14], BIDI-MIN[15], OCN[16], Nostrum[19, 20], Nexus[21], Xpipes[22], R2NoC[23], An Architecture and compiler for aSoC[24], DyAD[33], Mango[38-40], Wolkotte et. al.[41], Arteris[45], Kavaldjiev et. al.[51], DSPIN[52], TTNoC[68], NocMaker[69], UT TRIPS[71], Intel TeraFLOPS[72], EVC[85], Aelite[88], HT-OCTAGON[89], XHiNoC[90], RAMPSoC[94], DRNoC[95], Dynamic Reconfigurable Network on Chip[97], Ramos et. al. [98], Kilo-NoC[100], dAElite[102], BMNoC[103], Custom Network on Chip Architecture[104], DANoC[105], RecMIN[110] and HELIX[113] are few architectures which provide simple communication between PE's.

3.2 Narrow cast connection

Connection between one source PE with one or multiple destination PE's is called narrowcast connection. In narrow cast connection the instruction initiated by the source is only executed by one destination PE. The instruction or data send by the source PE is acknowledged by the return message from destination PE. These connections are bi-directional [142].

3.3 Multi cast connection

Multicast connection is between one source PE with one or multiple destinations PE's such that the instruction/data issued by the source PE is duplicated and the copies are sent to every destination PE. No return messages are allowed from destination PE to source PE in multicast connections due to memory limitations. These connections are uni-directional [142]. These are the architectures which provide multicast connections; CHAIN[9], Æthereal[12], BIDI-MIN[15], Nostrum[19, 20], An Architecture and compiler for aSoC[24], Mango[38-40], HIBI[63], artNoC[81], CDMA NoC[82], EVC[85], Aelite[88], XHiNoC[90], DRNoC[95], Dynamic Reconfigurable Network on Chip[97], Kilo-NoC[100], WiNoC[101], dAElite[102] and BLOCON[112].

3.4 Broad cast communication and multipath routing

In broadcast communication, source PE can send the packets to every destination PE attached with it either directly or indirectly [3]. SPIN[3], Nexus[21] and TTNoC[68] are few architecture which support broadcast communication. Multipath routing uses multiple paths available to route packet from source to destination. CLICHÉ[1] provides multipath routing. Other NoC architectures have not provided any information regarding it.

4. Quality of Service (QoS):

Guaranteed throughput service (GT/GS) and Best-effort services (BE) are two broad categories of services provided in NoC [120]. Literature shows that most of the NoC architectures are offering BE or packet based QoS. While only few NoC architectures are offering (GT/GS) or both QoS.

4.1 Guaranteed throughput services (GT/GS)

In GS, the resources are reserved for particular instant of time to particular source and destination pair. In GS connection the bandwidth is reserved for guaranteeing the throughput to source destination pair. At times, GS connection can be expensive and it is not utilized properly. Mostly PE's sends the burst of data on these GS connections and then it remains silent for certain period of time. This leads to the underutilization of the communication link. That is why, BE services are also provided along with the GS connection to utilized the unused bandwidth. Video processing is the example of GS connection [12, 143]. Architectures which are providing GS based communication services are aSOC[5], OCTAGON[7], Nexus[21], QNoC[29], Spatial Division Multiplexing NoC[44], PNoC[56], Cross road interconnection architecture[62], HIBI[63], ProtoNoC[67], CDMA NoC[82], TTNoC[84], MoCSYS[87], Aelite[88] and dAElite[102].

4.2 Best-effort services (BE)

Best effort service does not reserve any resource rather it uses the bandwidth unused by the GS connection. BE connections do not provide any guarantee of the bandwidth. BE services connections use the resources efficiently because they are designed for average case scenario as compared to the GS worst case scenarios. Cache updates are the example of BE connections respectively. This implies that GS traffic are used for critical traffic case while BE traffic is used for non-critical traffic [12, 143]. One of the major drawback of the BE

services is its unpredictability [144]. CLICHÉ[1], SPIN[3], Dally et al.[2], MicroNetwork[6], PROTEO[8], CHAIN[9], RAW[10], HERMES[14], BIDI-MIN[15], OCN[16], SoCIN[17], Xpipes[22], R2NoC[23], RaSoC[28], NoCGen[31], Topology adaptive NoC[43], Arteris[45], A low latency router[50], INoC[53], XGFT[54], Low latency on chip network[58], GEXPolygon & GEXSpidergon[59], Low-Power Network on Chip[60], NocMaker[69], TILEPro64[70], UT TRIPS[71], Intel TeraFLOPS[72], SCC[76], MoCRes[77], Generalized de Bruijn Graph NoC[78], Polaris[79], EVC[85], ReNoC[86], HT-OCTAGON[89], XHiNoC[90], Network on Chip in a Three Dimensional[91], BiNoC [92], RAMPSoC[94], DRNoC[95], Dynamic Reconfigurable Network on Chip[97], Ramos et. al.[98], Kilo-NoC[100], WiNoC[101], Custom Network on Chip Architecture[104], DANoC[105], WaveSync[106], AdNoC[107], Mesh based NoC[109], RecMIN[110] and SWIFT[111] are few architectures which provide BE based communication.

4.3 GS and BE services

Router handles both the GS and BE services connections at the NoC. There is an arbitration unit at router which separates the GS and BE connections. The router reads the packet format which has a bit pattern which specifies whether this packet should be sent on GS or BE connections. These packet bits are set by the PE which generates the traffic [12, 145]. Another approach to provide GS and BE services in the NoC is using virtual channels. The high priority virtual channels are used for guaranteed throughput traffic while low priority virtual channels are assigned to BE traffic [146, 147]. There are some NoC architectures which provide both GS and BE based communication. They are Æthereal[12], SoCBUS[13], Nostrum[19, 20], µSpider[25], Spidergon[27], Asynchronous On chip network router with Quality of Service[35], Mango[38-40] Wolkotte et. al.[41], Asynchronous NoC Architecture[48], Kavaldjiev et. al.[51], DSPIN[52], artNoC[81] and ALPIN[93].

5. Switching techniques:

Switching techniques refers to control of messages (packets or flits) flow between routers in NoC. It helps the routing algorithm to avoid congestions and conflicts between routers. Circuit switching techniques do not require forwarding strategy as resources are already reserved for them. Packet switching requires forwarding strategy as it have to made decision on per node basis and it requires buffering. In packet switching flits are saved in the router before any routing decision. There are broadly three types of switching techniques, store and forward, virtual cut through and wormhole switching.

The buffering requirement of virtual cut through and store and forward technique is one packet as compared to few flits of wormhole switching. The design complexity of virtual cut through is high as compared to wormhole switching and store and forward technique. The cost (power consumption and area) of wormhole switching is lower as compared to virtual cut through and store and forward technique [144]. At low traffic rate virtual cut through technique has the same low latency as wormhole switching. While at high traffic load the virtual cut through has high throughput as store and forward technique [43]. It is a trade-off between buffering, design complexity and cost for the usages of these switching techniques. 5% NoC architectures are using store and forward flow control technique. While 9% and 48% NoC architectures are using virtual cut through and wormhole switching. This shows the trends in NoC architecture. Scientist and researchers are conscious about the area and latency requirements.

5.1 Store and forward

In store and forward as the name suggests that the packet is completely received at the router and then routing decision is made on it. This increases the latency of the packet and there is more storage requirement at the router [134]. Eclipse[11], R2NoC[23], A 0.13µm NoC[26], Black-Bus[36] and ProtoNoC[67] are few architectures which have store and forward flow control.

5.2 Virtual cut through

In virtual cut through flow control, the flit is forwarded to the next router when the neighbor router guarantees that complete packet can be saved. If there is no space in the neighbor router then the complete packet will be saved in that particular router. Virtual cut through router also need buffers to save the complete packet but it has less latency as compared to store and forward technique [14, 134, 144]. When no packets are blocked in the buffers than virtual cut through switching achieves the same latency as of wormhole switching technique in NoC [144]. NoC architectures which have virtual cut through as flow control technique are Star Connected OCN[18], Topology adaptive NoC[43], CoNoChi[61], ProtoNoC[67], MoCRes[77], MoCSYS[87], Kilo-NoC[100], Custom Network on Chip Architecture[104] and Aurora[108].

5.3 Wormhole switching

In wormhole technique packet is divided in to flits. Header, body and tail flits are three broad categories. Header flit contains the routing information while body flit contains the data which is to be transfer from source to destination. Tail flit terminates the communication by informing the routers and the destination. The buffer requirement for the wormhole switching is less as compared to other two techniques. Similarly, wormhole switching has less latency communication requirement as compared to store and forward and virtual cut through [12, 134]. In certain cases the routing and control information are also provided in the packet by allocating few control bits [22]. The drawback of this technique is that when the header flit is blocked in any router all the subsequent following flits of a packet in multiple routers are also blocked. This leads to the deadlock situation in the NoC [144]. Few architectures have separate control lines and other used flow of tokens for flow control between routers [41, 112].

CLICHÉ[1], Dally et al. [2], SPIN[3], OCTAGON[7], RAW[10], Æthereal[12], HERMES[14], BIDI-MIN[15], SoCIN[17], Xpipes[22], Spidergon[27], RaSoC[28], QNoC[29], NoCGen[31], Reconfigurable Network on Chip[32], DyAD[33], Asynchronous On chip network router with Quality of Service[35], Arteris[45], Asynchronous NoC Architecture[48], A low latency router[50], DSPIN[52], INoC[53], High Throughput NoC Architecture[55], Low latency on chip network[58], GEXPolygon &

GEXSpidergon[59], HIBI[63], On chip multimedia Applications[64], Dynamic reconfigurable NoC for adaptive reconfigurable MPSoC[65], Communication Architecture Optimization[66], ProtoNoC[67], TILEPro64[70], UT TRIPS[71], Intel TeraFLOPS[72], EIB on chip network[75], SCC[76], Generalized de Bruijn Graph NoC[78], Polaris[79], artNoC[81], CDMA NoC[82], A reconfigurable baseband platform based on Asynchronous NoC[83], HT-OCTAGON[89], XHiNoC[90], Network on Chip in a Three Dimensional[91], BiNoC[92], DRNoC[95], Dynamic Reconfigurable Network on Chip[97], WiNoC[101], BMNoC[103], DANoC[105], WaveSync[106], AdNoC[107] and Mesh based NoC[109] are architecture which have adopted wormhole switching as a flow control technique.

5.4 Buffer management

For buffer management between routers, architectures use credit based and share vc control techniques. These techniques help to avoid buffer overflow, packet drop and to have reliable communication between source and destination. At times both these techniques can be used together for controlling the access to the common link. Due to less communication overhead in the shared vc control technique, it consumes less area and power than credit based technique [38].

5.4.1 Credit based buffer management & flow control technique

Credit based flow control technique is employed between adjacent routers and between router and NI. It controls the flow of flits by incrementing and decrementing the credit counter. When ports send a flit it decrements the counter which shows that the port has just send the flit and output port is busy. When the adjacent router receives the flit it sends back the credit message to the router so that it can increase the credit counter. Whenever the credit counter of the output port reaches zero, it cannot send more flits to that particular port [148]. SPIN[3], µSpider[25], QNoC[29], Asynchronous on chip network router with Quality of Service[35], TILEPro64[70], UT TRIPS[71], A reconfigurable baseband platform based on Asynchronous NoC[83], Ramos et. al. [98], dAElite[102], BMNoC[103], WaveSync[106] and BLOCON[112] are few architectures which have credit based buffer management and flow control technique.

5.4.2 Share virtual channel (vc) control technique

In share vc control technique there is a share and un-share box counters at source and destination. Whenever a flit is send from the source queue the share box is locked. Now source is not allowed to send more flits until the flit is received at the destination. When the flit is reached at the destination it will toggle the latch of unshared box, which in return sends the unlock signal to shared box via unlock link. This way the source is able to send more flits at the network provided there is no deadlock [38]. Mango[38-40] NoC architecture have adopted the share vc buffer management and flow control technique.

CONCLUSION:

This paper reviews the NoC architectures based on the different parameters. These parameters are link sharing mechanism, routing algorithm, connection types, quality of service, switching technique and NoC clocking mechanism. We believe that this survey will help the research community to have quick glance on the NoC architectures and find the un-resolved issues and contribute further.

REFERENCES:

[1] Shashi Kumar, Axel Jantsch, J-P Soininen, Martti Forsell, Mikael Millberg, Johny Oberg, Kari Tiensyrja, and Ahmed Hemani, "A network on chip architecture and design methodology," in *VLSI, 2002. Proceedings. IEEE Computer Society Annual Symposium on*, 2002, pp. 105-112.

[2] William J Dally and Brian Towles, "Route packets, not wires: on-chip interconnection networks," in *Design Automation Conference, 2001. Proceedings*, 2001, pp. 684-689.

[3] Pierre Guerrier and Alain Greiner, "A generic architecture for on-chip packet-switched interconnections," in *Proceedings of the conference on Design, automation and test in Europe*, 2000, pp. 250-256.

[4] Luca Benini and Giovanni De Micheli, "Networks on chips: a new SoC paradigm," *Computer,* vol. 35, pp. 70-78, 2002.

[5] Jian Liang, Sriram Swaminathan, and Russell Tessier, "aSOC: A scalable, single-chip communications architecture," in *Parallel Architectures and Compilation Techniques, 2000. Proceedings. International Conference on*, 2000, pp. 37-46.

[6] Drew Wingard, "MicroNetwork-based integration for SOCs," in *Design Automation Conference, 2001. Proceedings*, 2001, pp. 673-677.

[7] Faraydon Karim, Anh Nguyen, and Sujit Dey, "An interconnect architecture for networking systems on chips," *IEEE micro,* vol. 22, pp. 36-45, 2002.

[8] D Siguenza-Tortosa and Jari Nurmi, "Proteo: a new approach to network-on-chip," in *IASTED International Conference on Communication Systems and Networks (CSN'02)*, 2002.

[9] John Bainbridge and Steve Furber, "Chain: a delay-insensitive chip area interconnect," *IEEE Micro,* vol. 22, pp. 16-23, 2002.

[10] Michael Bedford Taylor, Jason Kim, Jason Miller, David Wentzlaff, Fae Ghodrat, Ben Greenwald, Henry Hoffman, Paul Johnson, Jae-Wook Lee, and Walter Lee, "The Raw microprocessor: A computational fabric for software circuits and general-purpose programs," *Micro, IEEE,* vol. 22, pp. 25-35, 2002.

[11] Martti Forsell, "A scalable high-performance computing solution for networks on chips," *IEEE Micro,* vol. 22, pp. 46-55, 2002.

[12] Edwin Rijpkema, Kees Goossens, Andrei Rădulescu, John Dielissen, Jef van Meerbergen, Paul Wielage, and Erwin Waterlander, "Trade-offs in the design of a router with both guaranteed and best-effort services for networks on chip," *IEE Proceedings-Computers and Digital Techniques,* vol. 150, pp. 294-302, 2003.

[13] Daniel Wiklund and Dake Liu, "SoCBUS: switched network on chip for hard real time embedded

systems," in *Parallel and Distributed Processing Symposium, 2003. Proceedings. International*, 2003, p. 8 pp.

[14] Fernando Moraes, Ney Calazans, Aline Mello, Leandro Möller, and Luciano Ost, "HERMES: an infrastructure for low area overhead packet-switching networks on chip," *INTEGRATION, the VLSI journal*, vol. 38, pp. 69-93, 2004.

[15] Partha Pratim Pande, Cristian Grecu, André Ivanov, and Res Saleh, "High-throughput switch-based interconnect for future SoCs," in *System-on-Chip for Real-Time Applications, 2003. Proceedings. The 3rd IEEE International Workshop on*, 2003, pp. 304-310.

[16] Tomas Henriksson, Daniel Wiklund, and Dake Liu, "VLSI implementation of a switch for on-chip networks," in *Proceedings of the International Workshop on Design and Diagnostics of Electronic Circuits and Systems, Poznan, Poland*, 2003.

[17] Cesar Albenes Zeferino and Altamiro Amadeu Susin, "SoCIN: a parametric and scalable network-on-chip," in *Integrated Circuits and Systems Design, 2003. SBCCI 2003. Proceedings. 16th Symposium on*, 2003, pp. 169-174.

[18] Se-Joong Lee, Seong-Jun Song, Kangmin Lee, Jeong-Ho Woo, Sung-Eun Kim, Byeong-Gyu Nam, and Hoi-Jun Yoo, "An 800MHz star-connected on-chip network for application to systems on a chip," in *Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE International*, 2003, pp. 468-469.

[19] Sandro Penolazzi and Axel Jantsch, "A high level power model for the Nostrum NoC," in *Digital System Design: Architectures, Methods and Tools, 2006. DSD 2006. 9th EUROMICRO Conference on*, 2006, pp. 673-676.

[20] Mikael Millberg, Erland Nilsson, Rikard Thid, and Axel Jantsch, "Guaranteed bandwidth using looped containers in temporally disjoint networks within the Nostrum network on chip," in *Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings*, 2004, pp. 890-895.

[21] Andrew Lines, "Asynchronous interconnect for synchronous SoC design," *Micro, IEEE*, vol. 24, pp. 32-41, 2004.

[22] Davide Bertozzi and Luca Benini, "Xpipes: a network-on-chip architecture for gigascale systems-on-chip," *Circuits and Systems Magazine, IEEE*, vol. 4, pp. 18-31, 2004.

[23] Henrik Samuelsson and Shashi Kumar, "Ring road NoC architecture," in *Norchip Conference, 2004. Proceedings*, 2004, pp. 16-19.

[24] Jian Liang, Andrew Laffely, Sriram Srinivasan, and Russell Tessier, "An architecture and compiler for scalable on-chip communication," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 12, pp. 711-726, 2004.

[25] Samuel Evain, J-P Diguet, and Dominique Houzet, "μ spider: a CAD tool for efficient NoC design," in *Norchip Conference, 2004. Proceedings*, 2004, pp. 218-221.

[26] Filippo Mondinelli, Michele Borgatti, and Zsolt M KOVACS VAJNA, "A 0.13 um 1Gb/s/channel store-and-forward network on-chip," in *IEEE Systems-on-chip conference*, 2004, pp. 141-142.

[27] Marcello Coppola, Riccardo Locatelli, Giuseppe Maruccia, Lorenzo Pieralisi, and Alberto Scandurra, "Spidergon: a novel on-chip communication network," in *System-on-Chip, 2004. Proceedings. 2004 International Symposium on*, 2004, p. 15.

[28] Cesar Albenes Zeferino, Márcio Eduardo Kreutz, and Altamiro Amadeu Susin, "RASoC: A router soft-core for networks-on-chip," in *Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings*, 2004, pp. 198-203.

[29] Evgeny Bolotin, Israel Cidon, Ran Ginosar, and Avinoam Kolodny, "QNoC: QoS architecture and design process for network on chip," *Journal of systems architecture*, vol. 50, pp. 105-128, 2004.

[30] Lee Kangmin, Lee Se-Joong, Kim Sung-Eun, Choi Hye-Mi, Kim Donghyun, Kim Sunyoung, Lee Min-Wuk, and Yoo Hoi-Jun, "A 51mW 1.6GHz on-chip network for low-power heterogeneous SoC platform," in *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International*, 2004, pp. 152-518 Vol.1.

[31] Jeremy Chan and Sri Parameswaran, "NoCGEN: A template based reuse methodology for networks on chip architecture," in *VLSI Design, 2004. Proceedings. 17th International Conference on*, 2004, pp. 717-720.

[32] Doris Ching, Patrick Schaumont, and Ingrid Verbauwhede, "Integrated modelling and generation of a reconfigurable network-on-chip," *International Journal of Embedded Systems*, vol. 1, pp. 218-227, 2005.

[33] Jingcao Hu and Radu Marculescu, "DyAD: smart routing for networks-on-chip," in *Proceedings of the 41st annual Design Automation Conference*, 2004, pp. 260-263.

[34] Hsin-Chou Chi and Jia-Hung Chen, "Design and implementation of a routing switch for on-chip interconnection networks," in *Advanced System Integrated Circuits 2004. Proceedings of 2004 IEEE Asia-Pacific Conference on*, 2004, pp. 392-395.

[35] F Feliciian and Stephen B Furber, "An asynchronous on-chip network router with quality-of-service (QoS) support," in *SOC Conference, 2004. Proceedings. IEEE International*, 2004, pp. 274-277.

[36] Kenichiro Anjo, Yutaka Yamada, Michihiro Koibuchi, Akiya Jouraku, and Hideharu Amano, "BLACK-BUS: a new data-transfer technique using local address on networks-on-chips," in *Parallel and Distributed Processing Symposium, 2004. Proceedings. 18th International*, 2004, p. 10.

[37] Sanghun Lee, Chanho Lee, and Hyuk-Jae Lee, "A new multi-channel on-chip-bus architecture for system-on-chips," in *SOC Conference, 2004. Proceedings. IEEE International*, 2004, pp. 305-308.

[38] Tobias Bjerregaard and Jens Sparso, "A router architecture for connection-oriented service guarantees in the MANGO clockless network-on-chip," in *Design,*

Automation and Test in Europe, 2005. Proceedings, 2005, pp. 1226-1231.

[39] Tobias Bjerregaard and Jens Sparso, "Virtual channel designs for guaranteeing bandwidth in asynchronous network-on-chip," in *Norchip Conference, 2004. Proceedings*, 2004, pp. 269-272.

[40] Tobias Bjerregaard and Jens Sparsø, "Scheduling discipline for latency and bandwidth guarantees in asynchronous network-on-chip," in *Asynchronous Circuits and Systems, 2005. ASYNC 2005. Proceedings. 11th IEEE International Symposium on*, 2005, pp. 34-43.

[41] Pascal T Wolkotte, Gerard JM Smit, Gerard K Rauwerda, and Lodewijk T Smit, "An energy-efficient reconfigurable circuit-switched network-on-chip," in *Parallel and Distributed Processing Symposium, 2005. Proceedings. 19th IEEE International*, 2005, pp. 155a-155a.

[42] Manish Amde, Tomaz Felicijan, Aristeidis Efthymiou, Douglas Edwards, and Luciano Lavagno, "Asynchronous on-chip networks," in *Computers and Digital Techniques, IEE Proceedings-*, 2005, pp. 273-283.

[43] TA Bartic, J-Y Mignolet, Vincent Nollet, Theodore Marescaux, Diederik Verkest, Serge Vernalde, and Rudy Lauwereins, "Topology adaptive network-on-chip design and implementation," *IEE Proceedings-Computers and Digital Techniques*, vol. 152, pp. 467-472, 2005.

[44] Anthony Leroy, Paul Marchal, Adelina Shickova, Francky Catthoor, Frédéric Robert, and Diederik Verkest, "Spatial division multiplexing: a novel approach for guaranteed throughput on NoCs," in *Proceedings of the 3rd IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis*, 2005, pp. 81-86.

[45] Swati Sharma, Chandra Mukherjee, and Ashish Gambhir, "A Comparison of Network-on-chip and Buses."

[46] Christophe Bobda, Ali Ahmadinia, Mateusz Majer, Jürgen Teich, Sándor Fekete, and Jan van der Veen, "Dynoc: A dynamic infrastructure for communication in dynamically reconfugurable devices," in *Field Programmable Logic and Applications, 2005. International Conference on*, 2005, pp. 153-158.

[47] Daewook Kim, Manho Kim, and Gerald E Sobelman, "Design of a high-performance scalable CDMA router for on-chip switched networks," *Memory*, vol. 8, p. 01100110, 2005.

[48] Edith Beigné, Fabien Clermidy, Pascal Vivet, Alain Clouard, and Marc Renaudin, "An asynchronous NOC architecture providing low latency service and its multi-level design framework," in *Asynchronous Circuits and Systems, 2005. ASYNC 2005. Proceedings. 11th IEEE International Symposium on*, 2005, pp. 54-63.

[49] Se-Joong Lee, Kwanho Kim, Hyejung Kim, Namjun Cho, and Hoi-Jun Yoo, "Adaptive network-on-chip with wave-front train serialization scheme," in *VLSI Circuits, 2005. Digest of Technical Papers. 2005 Symposium on*, 2005, pp. 104-107.

[50] Jongman Kim, Dongkook Park, Theo Theocharides, Narayanan Vijaykrishnan, and Chita R Das, "A low latency router supporting adaptivity for on-chip interconnects," in *Proceedings of the 42nd annual Design Automation Conference*, 2005, pp. 559-564.

[51] Nikolay Kavaldjiev, Gerard JM Smit, Pierre G Jansen, and Pascal T Wolkotte, "A Virtual Channel Network-on-Chip for GT and BE traffic," in *Emerging VLSI Technologies and Architectures, 2006. IEEE Computer Society Annual Symposium on*, 2006, p. 6 pp.

[52] I Miro Panades, Alain Greiner, Abbas Sheibanyrad, and G STMicroelcctronics, "A low cost network-on-chip with guaranteed service well suited to the GALS approach," *Proc. NANONET*, 2006.

[53] Christian Neeb and Norbert Wehn, "Designing efficient irregular networks for heterogeneous systems-on-chip," *Journal of Systems architecture*, vol. 54, pp. 384-396, 2008.

[54] Heikki Kariniemi and Jari Nurmi, "On-Line Reconfigurable XGFT Network-on-Chip Designed for Improving the Fault-Tolerance and Manufacturability of the MPSoC Chips," in *Field Programmable Logic and Applications, 2006. FPL'06. International Conference on*, 2006, pp. 1-6.

[55] A Bouhraoua and ME Elrabaa, "A high-throughput network-on-chip architecture for systems-on-chip interconnect," in *System-on-Chip, 2006. International Symposium on*, 2006, pp. 1-4.

[56] Clint Hilton and Brent Nelson, "PNoC: a flexible circuit-switched NoC for FPGA-based systems," *IEE Proceedings-Computers and Digital Techniques*, vol. 153, pp. 181-188, 2006.

[57] Azeez Sanusi and Magdy A. Bayoumi Nan Wang, "A Central Caching Network-on-chip Communication Architecture Design," 2006.

[58] Robert Mullins, Andrew West, and Simon Moore, "The design and implementation of a low-latency on-chip network," in *Proceedings of the 2006 Asia and South Pacific Design Automation Conference*, 2006, pp. 164-169.

[59] M Zid, A Zitouni, A Baganne, and R Tourki, "New generic gals noc architectures with multiple qos," in *Design and Test of Integrated Systems in Nanoscale Technology, 2006. DTIS 2006. International Conference on*, 2006, pp. 345-349.

[60] Kangmin Lee, Se-Joong Lee, and Hoi-Jun Yoo, "Low-power network-on-chip for high-performance SoC design," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 14, pp. 148-160, 2006.

[61] Thilo Pionteck, Roman Koch, and Carsten Albrecht, "Applying partial reconfiguration to networks-on-chips," in *Field Programmable Logic and Applications, 2006. FPL'06. International Conference on*, 2006, pp. 1-6.

[62] Kuei-Chung Chang, Jih-Sheng Shen, and Tien-Fu Chen, "Evaluation and design trade-offs between circuit-switched and packet-switched NOCs for application-specific SOCs," in *Proceedings of the 43rd annual Design Automation Conference*, 2006, pp. 143-

148.

[63] Erno Salminen, Tero Kangas, Timo D Hämäläinen, Jouni Riihimäki, Vesa Lahtinen, and Kimmo Kuusilinna, "HIBI communication network for system-on-chip," *Journal of VLSI signal processing systems for signal, image and video technology*, vol. 43, pp. 185-205, 2006.

[64] Hyung Gyu Lee, Umit Y Ogras, Radu Marculescu, and Naehyuck Chang, "Design space exploration and prototyping for on-chip multimedia applications," in *Proceedings of the 43rd annual Design Automation Conference*, 2006, pp. 137-142.

[65] Balal Ahmad, Ahmet T Erdogan, and Sami Khawam, "Architecture of a dynamically reconfigurable NoC for adaptive reconfigurable MPSoC," in *Adaptive Hardware and Systems, 2006. AHS 2006. First NASA/ESA Conference on*, 2006, pp. 405-411.

[66] Umit Y Ogras, Radu Marculescu, Hyung Gyu Lee, and Naehyuck Chang, "Communication architecture optimization: making the shortest path shorter in regular networks-on-chip," in *Proceedings of the conference on Design, automation and test in Europe: Proceedings*, 2006, pp. 712-717.

[67] David Castells-Rufas, Jaume Joven, and Jordi Carrabina, "A validation and performance evaluation tool for ProtoNoc," in *System-on-Chip, 2006. International Symposium on*, 2006, pp. 1-4.

[68] Martin Schoeberl, "A time-triggered network-on-chip," in *Field Programmable Logic and Applications, 2007. FPL 2007. International Conference on*, 2007, pp. 377-382.

[69] David Castells-Rufas, Jaume Joven, Sergi Risueño, Eduard Fernandez, and Jordi Carrabina, "NocMaker: A cross-platform open-source design space exploration tool for networks on chip," in *INA-OCMC Workshop, Paphos, Cyprus*, 2009.

[70] Shane Bell, Bruce Edwards, John Amann, Rich Conlin, Kevin Joyce, Vince Leung, John MacKay, Mike Reif, Liewei Bao, and John Brown, "Tile64-processor: A 64-core soc with mesh interconnect," in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, 2008, pp. 88-598.

[71] Paul Gratz, Changkyu Kim, Karthikeyan Sankaralingam, Heather Hanson, Premkishore Shivakumar, Stephen W Keckler, and Doug Burger, "On-chip interconnection networks of the TRIPS chip," *Micro, IEEE*, vol. 27, pp. 41-50, 2007.

[72] Sriram R Vangal, Jason Howard, Gregory Ruhl, Saurabh Dighe, Howard Wilson, James Tschanz, David Finan, Arvind Singh, Tiju Jacob, and Shailendra Jain, "An 80-tile sub-100-w teraflops processor in 65-nm cmos," *Solid-State Circuits, IEEE Journal of*, vol. 43, pp. 29-41, 2008.

[73] Mike Butts, "Synchronization through communication in a massively parallel processor array," *Micro, IEEE*, vol. 27, pp. 32-40, 2007.

[74] Gianluca Palermo, Cristina Silvano, Giovanni Mariani, Riccardo Locatelli, and Marcello Coppola, "Application-specific topology design customization for stnoc," in *Digital System Design Architectures, Methods and Tools, 2007. DSD 2007. 10th Euromicro Conference on*, 2007, pp. 547-550.

[75] Thomas William Ainsworth and Timothy Mark Pinkston, "Characterizing the Cell EIB on-chip network," *Micro, IEEE*, vol. 27, pp. 6-14, 2007.

[76] Jeff Hoffman, David Arditti Ilitzky, Anthony Chun, and Aliaksei Chapyzhenka, "Architecture of the scalable communications core," in *Proceedings of the First International Symposium on Networks-on-Chip*, 2007, pp. 40-52.

[77] Arun Janarthanan, Vijay Swaminathan, and Karen A Tomko, "MoCReS: an Area-Efficient Multi-Clock On-Chip Network for Reconfigurable Systems," in *VLSI, 2007. ISVLSI'07. IEEE Computer Society Annual Symposium on*, 2007, pp. 455-456.

[78] Mohammad Hosseinabady, Mohammad Reza Kakoee, Jimson Mathew, and Dhiraj K Pradhan, "Reliable network-on-chip based on generalized de Bruijn graph," in *High Level Design Validation and Test Workshop, 2007. HLVDT 2007. IEEE International*, 2007, pp. 3-10.

[79] Vassos Soteriou, Noel Eisley, Hangsheng Wang, Bin Li, and Li-Shiuan Peh, "Polaris: A system-level roadmap for on-chip interconnection networks," in *Computer Design, 2006. ICCD 2006. International Conference on*, 2007, pp. 134-141.

[80] Lars Braun, M Hubner, Jürgen Becker, Thomas Perschke, Volker Schatz, and Stefan Bach, "Circuit switched run-time adaptive network-on-chip for image processing applications," in *Field Programmable Logic and Applications, 2007. FPL 2007. International Conference on*, 2007, pp. 688-691.

[81] Christian Schuck, Stefan Lamparth, and Jürgen Becker, "artNoC-A novel multi-functional router architecture for Organic Computing," in *Field Programmable Logic and Applications, 2007. FPL 2007. International Conference on*, 2007, pp. 371-376.

[82] Xin Wang, Tapani Ahonen, and Jari Nurmi, "Applying CDMA technique to network-on-chip," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 15, pp. 1091-1100, 2007.

[83] Didier Lattard, Edith Beigne, Fabien Clermidy, Yves Durand, Romain Lemaire, Pascal Vivet, and Friedbert Berens, "A reconfigurable baseband platform based on an asynchronous network-on-chip," *Solid-State Circuits, IEEE Journal of*, vol. 43, pp. 223-235, 2008.

[84] Christian Paukovits and Hermann Kopetz, "Concepts of switching in the time-triggered network-on-chip," in *Embedded and Real-Time Computing Systems and Applications, 2008. RTCSA'08. 14th IEEE International Conference on*, 2008, pp. 120-129.

[85] Amit Kumar, Li-Shiuan Peh, Partha Kundu, and Niraj K Jha, "Toward ideal on-chip communication using express virtual channels," *IEEE micro*, vol. 28, pp. 80-90, 2008.

[86] Mikkel Bystrup Stensgaard and Jens Sparso, "Renoc: A network-on-chip architecture with reconfigurable topology," in *Networks-on-Chip, 2008. NoCS 2008. Second ACM/IEEE International Symposium on*, 2008,

pp. 55-64.

[87] Arun Janarthanan and Karen A Tomko, "MoCSYS: A Multi-Clock Hybrid Two-Layer Router Architecture and Integrated Topology Synthesis Framework for System-Level Design of FPGA Based On-Chip Networks," in *VLSI Design, 2008. VLSID 2008. 21st International Conference on*, 2008, pp. 397-402.

[88] Andreas Hansson, Mahesh Subburaman, and Kees Goossens, "aelite: A flit-synchronous network on chip with composable and predictable services," in *Proceedings of the conference on design, automation and test in Europe*, 2009, pp. 250-255.

[89] MA Abd El Ghany, Magdy A El-Moursy, Darek Korzec, and Mohammed Ismail, "High throughput architecture for OCTAGON network on chip," in *Electronics, Circuits, and Systems, 2009. ICECS 2009. 16th IEEE International Conference on*, 2009, pp. 101-104.

[90] Faizal A Samman, Thomas Hollstein, and Manfred Glesner, "Networks-on-chip based on dynamic wormhole packet identity mapping management," *VLSI Design*, vol. 2009, p. 2, 2009.

[91] Brett Stanley Feero and Partha Pratim Pande, "Networks-on-chip in a three-dimensional environment: A performance evaluation," *Computers, IEEE Transactions on*, vol. 58, pp. 32-45, 2009.

[92] Ying-Cherng Lan, Hsiao-An Lin, Shih-Hsin Lo, Yu Hen Hu, and Sao-Jie Chen, "A bidirectional NoC (BiNoC) architecture with dynamic self-reconfigurable channel," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 30, pp. 427-440, 2011.

[93] Edith Beigné, Fabien Clermidy, Hélène Lhermet, Sylvain Miermont, Yvain Thonnart, Xuan-Tu Tran, Alexandre Valentian, Didier Varreau, Pascal Vivet, and Xavier Popon, "An asynchronous power aware and adaptive NoC based circuit," *Solid-State Circuits, IEEE Journal of*, vol. 44, pp. 1167-1177, 2009.

[94] D Gohringer, M Hubner, Laure Hugot-Derville, and Jürgen Becker, "Message passing interface support for the runtime adaptive multi-processor system-on-chip RAMPSoC," in *Embedded Computer Systems (SAMOS), 2010 International Conference on*, 2010, pp. 357-364.

[95] Yana E Krasteva, Eduardo De la Torre, and Teresa Riesgo, "Reconfigurable networks on chip: DRNoC architecture," *Journal of Systems Architecture*, vol. 56, pp. 293-302, 2010.

[96] Nan Wang, Azeez Sanusi, PY Zhao, M Elgamel, and Magdy A Bayoumi, "PMCNOC: A pipelining multi-channel central caching network-on-chip communication architecture design," *Journal of Signal Processing Systems*, vol. 60, pp. 315-331, 2010.

[97] Li-Wei Wu, Wei-Xiang Tang, and Yarsun Hsu, "A novel architecture and routing algorithm for dynamic reconfigurable network-on-chip," in *Parallel and Distributed Processing with Applications (ISPA), 2011 IEEE 9th International Symposium on*, 2011, pp. 177-182.

[98] JC Peña-Ramos and Ramon Parra-Michel, "Network on Chip Architectures for High Performance Digital Signal Processing Using a Configurable Core," in *Reconfigurable Computing and FPGAs (ReConFig), 2011 International Conference on*, 2011, pp. 375-379.

[99] Sébastien Le Beux, Jelena Trajkovic, Ian O'Connor, Gabriela Nicolescu, Guy Bois, and Pierre Paulin, "Optical ring network-on-chip (ORNoC): Architecture and design methodology," in *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2011*, 2011, pp. 1-6.

[100] Boris Grot, Joel Hestness, Stephen W Keckler, and Onur Mutlu, "Kilo-NOC: a heterogeneous network-on-chip architecture for scalability and service guarantees," *ACM SIGARCH Computer Architecture News*, vol. 39, pp. 401-412, 2011.

[101] Amlan Ganguly, Kevin Chang, Sujay Deb, Partha Pratim Pande, Benjamin Belzer, and Christof Teuscher, "Scalable hybrid wireless network-on-chip architectures for multicore systems," *Computers, IEEE Transactions on*, vol. 60, pp. 1485-1502, 2011.

[102] Radu Andrei Stefan, Anca Molnos, and Kees Goossens, "daelite: A tdm noc supporting qos, multicast, and fast connection set-up," *Computers, IEEE Transactions on*, vol. 63, pp. 583-594, 2014.

[103] Seungju Lee, Nozomu Togawa, Yusuke Sekihara, Takashi Aoki, and Akira Onozawa, "A hybrid NoC architecture utilizing packet transmission priority control method," in *Circuits and Systems (APCCAS), 2012 IEEE Asia Pacific Conference on*, 2012, pp. 404-407.

[104] P. Mishra, A. Nidhi, and J. K. Kishore, "Custom Network on Chip architecture for map generation in autonomous navigating robots," in *India Conference (INDICON), 2012 Annual IEEE*, 2012, pp. 086-091.

[105] Hao Shu, Jiang-Yi Shi, Yue Hao, Pei-Jun Ma, and Zhao Xu, "Danoc: a dynamic adaptive network on chip architecture," in *Solid-State and Integrated Circuit Technology (ICSICT), 2012 IEEE 11th International Conference on*, 2012, pp. 1-3.

[106] Yoon Seok Yang, Reeshav Kumar, Gwan Choi, and Paul V Gratz, "WaveSync: Low-Latency Source-Synchronous Bypass Network-on-Chip Architecture," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 19, p. 34, 2014.

[107] Mohammad Abdullah Al Faruque, Thomas Ebi, and Jörg Henkel, "AdNoC: runtime adaptive network-on-chip architecture," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 20, pp. 257-269, 2012.

[108] Amer Qouneh, Zhongqi Li, Madhura Joshi, Wangyuan Zhang, Xin Fu, and Tao Li, "Aurora: A thermally resilient photonic network-on-chip architecture," in *Computer Design (ICCD), 2012 IEEE 30th International Conference on*, 2012, pp. 379-386.

[109] Sudhanshu Choudhary and Shafi Qureshi, "Performance evaluation of mesh-based NoCs: Implementation of a new architecture and routing algorithm," *International Journal of Automation and Computing*, vol. 9, pp. 403-413, 2012.

[110] Alexander Logvinenko, Carsten Gremzow, and

Dietmar Tutsch, "RecMIN: A reconfiguration architecture for network on chip," in *Reconfigurable and Communication-Centric Systems-on-Chip (ReCoSoC), 2013 8th International Workshop on*, 2013, pp. 1-6.

[111] Jacob Postman, Tushar Krishna, Christopher Edmonds, Li-Shiuan Peh, and Patrick Chiang, "Swift: A low-power network-on-chip implementing the token flow control router architecture with swing-reduced interconnects," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 21, pp. 1432-1446, 2013.

[112] Yu-Hsiang Kao and H Jonathan Chao, "Design of a bufferless photonic clos network-on-chip architecture," *Computers, IEEE Transactions on*, vol. 63, pp. 764-776, 2014.

[113] Shirish Bahirat and Sudeep Pasricha, "HELIX: Design and synthesis of hybrid nanophotonic application-specific network-on-chip architectures," in *Quality Electronic Design (ISQED), 2014 15th International Symposium on*, 2014, pp. 91-98.

[114] Tobias Bjerregaard and Shankar Mahadevan, "A survey of research and practices of network-on-chip," *ACM Computing Surveys (CSUR)*, vol. 38, p. 1, 2006.

[115] Erno Salminen, Ari Kulmala, and Timo D Hamalainen, "Survey of network-on-chip proposals," *white paper, OCP-IP*, pp. 1-13, 2008.

[116] Eduard Fernandez-Alonso, David Castells-Rufas,

[122] Chifeng Wang, Wen-Hsiang Hu, Seung Eun Lee, and Nader Bagherzadeh, "Area and power-efficient innovative congestion-aware Network-on-Chip architecture," *Journal of Systems Architecture*, vol. 57, pp. 24-38, 2011.

[123] Wei Song and Doug Edwards, "Asynchronous spatial division multiplexing router," *Microprocessors and Microsystems*, vol. 35, pp. 85-97, 2011.

[124] Maurizio Palesi and Masoud Daneshtalab, *Routing algorithms in networks-on-chip*: Springer, 2014.

[125] Sudeep Pasricha and Yong Zou, "A low overhead fault tolerant routing scheme for 3D Networks-on-Chip," in *Quality Electronic Design (ISQED), 2011 12th International Symposium on*, 2011, pp. 1-8.

[126] Haibo Zhu, Partha Pratim Pande, and Cristian Grecu, "Performance evaluation of adaptive routing algorithms for achieving fault tolerance in NoC fabrics," in *Application-specific Systems, Architectures and Processors, 2007. ASAP. IEEE International Conf. on*, 2007, pp. 42-47.

[127] Young Bok Kim and Yong-Bin Kim, "Fault tolerant source routing for network-on-chip," in *Defect and Fault-Tolerance in VLSI Systems, 2007. DFT'07. 22nd IEEE International Symposium on*, 2007, pp. 12-20.

[128] Timo Schonwald, Jochen Zimmermann, Oliver Bringmann, and Wolfgang Rosenstiel, "Fully adaptive fault-tolerant routing algorithm for network-on-chip architectures," in *Digital System Design Architectures, Methods and Tools, 2007. DSD 2007. 10th Euromicro Conference on*, 2007, pp. 527-534.

[129] Timo Schonwald, Oliver Bringmann, and Wolfgang Rosenstiel, "Region-based routing algorithm for

Jaume Joven, and Jordi Carrabina, "Survey of NoC and programming models proposals for MPSoC," *International Journal of Computer Science Issues*, vol. 9, pp. 22-32, 2012.

[117] Ankur Agarwal, Cyril Iskander, and Ravi Shankar, "Survey of network on chip (noc) architectures & contributions," *Journal of engineering, Computing and Architecture*, vol. 3, pp. 21-27, 2009.

[118] David Atienza, Federico Angiolini, Srinivasan Murali, Antonio Pullini, Luca Benini, and Giovanni De Micheli, "Network-on-Chip design and synthesis outlook," *INTEGRATION, the VLSI journal*, vol. 41, pp. 340-359, 2008.

[119] Umit Y Ogras, Jingcao Hu, and Radu Marculescu, "Key research problems in NoC design: a holistic perspective," in *Proceedings of the 3rd IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis*, 2005, pp. 69-74.

[120] Jari Nurmi, "Network-on-chip: A new paradigm for system-on-chip design," in *System-on-Chip, 2005. Proceedings. 2005 International Symposium on*, 2005, pp. 2-6.

[121] Partha Pratim Pande, Cristian Grecu, Michael Jones, Andre Ivanov, and Resve Saleh, "Performance evaluation and design trade-offs for network-on-chip interconnect architectures," *Computers, IEEE Transactions on*, vol. 54, pp. 1025-1040, 2005.

network-on-chip architectures," in *Norchip, 2007*, 2007, pp. 1-4.

[130] Christopher J Glass and Lionel M Ni, "The turn model for adaptive routing," in *25 years of the international symposia on Computer architecture (selected papers)*, 1998, pp. 441-450.

[131] Ge-Ming Chiu, "The odd-even turn model for adaptive routing," *Parallel and Distributed Systems, IEEE Transactions on*, vol. 11, pp. 729-738, 2000.

[132] Poona Bahrebar and Dirk Stroobandt, "Adaptive and reconfigurable fault-tolerant routing method for 2D networks-on-chip," in *International Conference on ReConFigurable Computing and FPGAs (ReConFig'14)*, 2014, pp. 1-8.

[133] Matthew Pirretti, Greg M Link, Richard R Brooks, Narayanan Vijaykrishnan, Mahmut Kandemir, and Mary Jane Irwin, "Fault tolerant algorithms for network-on-chip interconnect," in *VLSI, 2004. Proceedings. IEEE Computer society Annual Symposium on*, 2004, pp. 46-51.

[134] Ville Rantala, Teijo Lehtonen, and Juha Plosila, *Network on chip routing algorithms*: Citeseer, 2006.

[135] Muhammad Athar Javed Sethi, Fawnizu Azmadi Hussin, and Nor Hisham Hamid, "Implementation of biological sprouting algorithm for NoC fault tolerance," in *Circuits and Systems (ICCAS), 2013 IEEE International Conference on*, 2013, pp. 39-44.

[136] Muhammad Athar Javed Sethi, Fawnizu Azmadi Hussin, and Nor Hisham Hamid, "Synaptogenesis based bio-inspired NoC fault tolerant interconnects," in *Control System, Computing and Engineering (ICCSCE), 2013 IEEE International Conference on*,

2013, pp. 46-51.

[137] Jie Wu, "A fault-tolerant adaptive and minimal routing approach in nD meshes," in *Parallel Processing, 2000. Proceedings. 2000 International Conference on*, 2000, pp. 431-438.

[138] Andrew A Chien and Jae H Kim, "Planar-adaptive routing: low-cost adaptive networks for multiprocessors," *Journal of the ACM (JACM)*, vol. 42, pp. 91-123, 1995.

[139] Falko Dressler and Ozgur B Akan, "Bio-inspired networking: from theory to practice," *Communications Magazine, IEEE*, vol. 48, pp. 176-183, 2010.

[140] Mohamed Bakhouya, "Towards a bio-inspired architecture for autonomic network-on-chip," in *High Performance Computing and Simulation (HPCS), 2010 International Conference on*, 2010, pp. 491-497.

[141] M. A. J. Sethi, F. A. Hussin, and N. H. Hamid, "Bio-inspired NoC fault tolerant techniques," in *Intelligent and Advanced Systems (ICIAS), 2014 5th International Conference on*, 2014, pp. 1-6.

[142] Andrei Radulescu and Kees Goossens, "Communication services for networks on chip," *Domain-Specific Processors: Systems, Architectures, Modeling, and Simulation*, pp. 193-213, 2004.

[143] Kees Goossens, John Dielissen, and Andrei Radulescu, "Æthereal network on chip: concepts, architectures, and implementations," *Design & Test of Computers, IEEE*, vol. 22, pp. 414-421, 2005.

[144] Konstantinos Tatas, Kostas Siozios, Dimitrios Soudris, and Axel Jantsch, *Designing 2D and 3D Network-on-chip Architectures*: Springer, 2014.

[145] John Dielissen, Andrei Radulescu, Kees Goossens, and Edwin Rijpkema, "Concepts and implementation of the Philips network-on-chip," in *IP-Based SoC Design*, 2003, pp. 1-6.

[146] Nikolay Kavaldjiev, Gerard JM Smit, Pascal T Wolkotte, and Pierre G Jansen, "Providing QoS guarantees in a NoC by virtual channel reservation," in *Reconfigurable Computing: Architectures and Applications*, ed: Springer, 2006, pp. 299-310.

[147] Rostislav Reuven Dobkin, Ran Ginosar, and Israel Cidon, "Qnoc asynchronous router with dynamic virtual channel allocation," in *Proceedings of the First International Symposium on Networks-on-Chip*, 2007, p. 218.

[148] Andreas Hansson, Kees Goossens, and Andrei Rădulescu, "Avoiding message-dependent deadlock in network-based systems on chip," *VLSI design*, vol. 2007, 2007.