

DIGITAL PHASE-SENSITIVE DETECTOR (PSD) AS ACCUMULATOR-SAMPLER AND ITS IMPLEMENTATION IN FPGA

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ABSTRACT: Phase-sensitive detection (PSD) is an established measurement technique for noisy signals. More recently, digital implementation of PSD using FPGA (Field Programmable Gate Array) or processor is becoming norm. This paper presents an FPGA-based digital PSD system, which is incorporated in a multi-channel bio-medical EIT instrument. In the paper, digital PSD has been analyzed using time- and frequency-domain methods of signal processing theory and a new interpretation of digital PSD in terms of accumulator-sampler has been given. Regarding design and implementation of the FPGA-based digital PSD system, two important issues of number of digitized waveform samples for use in PSD calculation and finite word length effect on PSD precision have been explored. Test results of the EIT instrument incorporating this digital PSD system have shown good noise performance, achieving an overall SNR of almost 80 dB at the high data-capturing rate of 100 frames/sec. The instrument also showed measurement capability to resolve large conductivity changes over very small spatial regions.

Key Words: accumulator, FPGA, matched filter, noise, precision, PSD, SNR

1. INTRODUCTION

Phase-Sensitive detection (PSD) is a technique used in instrumentation and measurement systems, to extract the characteristic(s) of a signal buried in noise [1]. This technique is used in, for example, electrical impedance tomography (EIT) systems [2] to recover the amplitude and phase information of the measured sinusoidal voltage signal, which could be buried in random noise. PSD also has other names in the literature, such as lock-in detection, synchronous detection and coherent/balanced demodulation. Mathematically, PSD is a special case of the correlation principle [1].

ANALOGUE AND DIGITAL PSD

Traditionally, an analogue PSD circuit (figure 1) comprises a switching amplifier (whose gain is switched between +B and -B) followed by a low-pass filter [3,4]. Switching of the amplifier gain is controlled by a reference signal having the same frequency (f_c) as that of the input signal, V_{in} , whose amplitude A is the information to be extracted. The two signals, input and reference, have to be phase-locked, with phase difference ϕ , which would not necessarily be zero. The switching amplifier effectively acts as a synchronous full-wave rectifier for V_{in} , or as an analogue multiplier multiplying the input signal V_{in} with the square-wave reference signal. The low-pass filter, following the switching amplifier, extracts V_{out} , the dc component of the amplifier's output signal.

The main disadvantage of the switching-based analogue PSD is that the odd harmonic components present in the square-wave signal can be potentially down-converted to dc and subsequently added into the otherwise correct dc component at the amplifier output, hence causing an error. For its resolution, modified version of analogue PSD uses analogue multiplier instead of switching amplifier with the

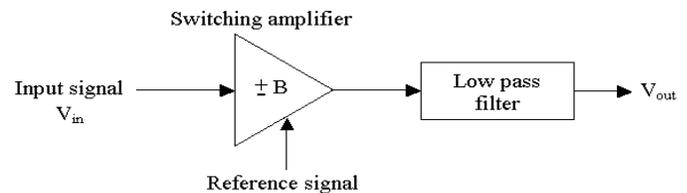


Fig. 1 Block diagram of an analogue PSD circuit

reference signal being a sinusoid instead of square-wave. Its close counterpart is the analogue matched filter, in which an analogue multiplier, having sinusoidal reference and the measured signal as the two inputs, is followed by an integrator-sampler [5]. The analogue matched filter provides maximum SNR improvement when detecting signals in Gaussian noise [2].

It can be shown mathematically that V_{out} for both types of analogue PSD mentioned above is proportional to $AB \cos\phi$. This PSD result can be interpreted and utilised in many ways. For example, if ϕ is known and/or constant, then this output dc value is proportional to the amplitude information (A) of the input signal, as B is known beforehand. On the other hand, if A is known and/or constant, then this output dc value is proportional to the cosine of the phase difference between the input and reference signals. Furthermore, this output dc value is proportional to that component of the input signal which is in phase with the reference signal; hence the term in-phase (I) component $V_{out,I}$.

In cases where both A and ϕ are unknown and varying, then another PSD result is required. Thus, another PSD circuit, using a reference signal shifted by 90° from previous I-case, is used. This gives an output of the low-pass filter which would be proportional to $AB \sin\phi$. It is called quadrature-phase (Q) component $V_{out,Q}$. These two PSD circuits make up what is called an I/Q demodulator and,

using their two dc output values $V_{out,I}$ and $V_{out,Q}$, both the amplitude (A) and phase (ϕ) information of the input signal V_{in} is calculated.

The use of analogue PSD, of both gain-switching and analogue-multiplier types, has problems [3, 6] in terms of noise, dc offset error, inaccurate matching of the I and Q arms of the I/Q demodulator, limited rejection by the analogue low-pass filter, harmonic distortion etc. With the development of technology, digital alternatives of analogue matched filtering and analogue PSD started appearing, e.g. [7, 8]. It was proposed that the digital matched filter would provide an improvement in SNR over the analogue matched filter and a digital demodulator based on matched filter theory would give the best SNR, besides being easy to modify [3, 5]. This triggered the use of digital PSD in the forthcoming EIT systems, which has now become a steady trend, e.g. [2,9] and [10, 11] have used DSP, Microprocessor and FPGA chips respectively to implement digital PSD. With the growth of the dsp techniques, digital PSD is now frequently implemented in the wide-ranging areas of instrumentation and tomography; see [12-16]. Recently, a new digital PSD system of switching type has been proposed [17].

In the case of digital PSD, the two dc outputs $V_{out,I}$ and $V_{out,Q}$ can be shown mathematically as in equations 1 and 2. The constant K would represent the overall scaling factor as the analogue voltage actually measured is processed through each of the I and Q arms to ultimately reach the output of the low-pass filter.

$$V_{out,I} = \frac{KAB\cos\phi}{2} \quad (1)$$

$$V_{out,Q} = \frac{KAB\sin\phi}{2} \quad (2)$$

These two dc output values can be used to calculate the amplitude (A) and phase (ϕ) of the input signal.

This paper presents a digital PSD system implemented in FPGA. This digital PSD system has been incorporated in each of the 35 parallel voltage-measurement channels of the bio-medical EIT instrument fEITER (functional Electrical Impedance Tomography of Evoked Responses) built at the University of Manchester [11]. The aim of fEITER is to achieve brain function imaging at sub-second time-scales, with the measurement sensitivity of around 80 dB at the high data-capturing rate of 100 frames/sec. Firmware loaded on a Xilinx Virtex-4 SX35 FPGA performs the EIT operation, including the PSD calculation. Design and implementation of this FPGA-based PSD system are discussed in Sections 3 and 4.

2. TIME- AND FREQUENCY-DOMAIN ANALYSIS OF DIGITAL PSD

This section presents time- and frequency-domain analysis of digital PSD using a Matlab-based example. The simulated

signal used here for PSD calculation is similar to the measured signal of the practically-implemented FPGA-based system.

Following two digital PSD equations respectively are used to implement the I and Q arms of the I/Q demodulator, in a processor or FPGA chip.

$$z_I = \sum_{n=0}^{L-1} x_{RefSine}[n] \cdot s[n] \quad (3)$$

$$z_Q = \sum_{n=0}^{L-1} x_{RefCos}[n] \cdot s[n] \quad (4)$$

where L is the number of samples of these signals being used in PSD. In this example, value of L is 200. The signals $y_{RefSine}[n]$ and $y_{RefCosine}[n]$, the in-phase and quadrature-phase reference signals, are sinusoids of frequency 10 kHz, sampled at 500 kS/s and occupying the dynamic range of 16 bits, as in the practically implemented digital PSD system discussed later.

$$y_{RefSine}[n] = \begin{cases} 32767 \times \sin\left(2\pi n \left(\frac{10}{500}\right)\right) & 0 \leq n \leq 199 \\ 0 & \text{else n} \end{cases} \quad (5)$$

$$y_{RefCos}[n] = \begin{cases} 32767 \times \cos\left(2\pi n \left(\frac{10}{500}\right)\right) & 0 \leq n \leq 199 \\ 0 & \text{else n} \end{cases} \quad (6)$$

The signal $s[n]$ is the digitised form of the phase-shifted and dc-level-shifted sinusoidal signal of frequency 10 kHz sampled at 500 kS/s (such as the one coming from a unipolar ADC).

$$s[n] = \begin{cases} A_{dc} + G \sin\left(2\pi n \left(\frac{10}{500}\right) + \Phi\right) & 0 \leq n \leq 199 \\ 0 & \text{else n} \end{cases} \quad (7)$$

where:

The dc level of the digitised sinusoid, $A_{dc} = 32768$

Amplitude of the digitised sinusoid, $G = 16384$

Phase-shift in the sinusoid, $\Phi = \pi / 3$

A time- and frequency-domain based analysis of the PSD process involving these signals follows.

Having L samples of these three signals is equivalent to implementing windowing i.e. time-domain multiplication of the three sinusoidal signals of frequency 10 kHz, with rectangular time-window function. As a result, the frequency spectrum of the rectangular time-window function is shifted

to 10 kHz. In the frequency spectrum of this up-shifted function, the centre peak-to-null width of the main lobe [18] is given by

$$\text{Main lobe width (peak-to-null)} = \frac{2}{L} \times \text{Nyquist Frequency} \tag{8}$$

For window length L of 200 and Nyquist frequency of 250 kHz (corresponding to the sampling rate of 500 kS/s), this main lobe width is 2.5 kHz. Ideally, this bandwidth should be as small as possible. This would mean larger L, consequently increasing the ‘cost’ of digital implementation of PSD, as more number of samples would need to be processed.

In the PSD process, two product sequences $p_I[n]$ and $p_Q[n]$ are calculated thus:

$$p_I[n] = y_{\text{RefSine}}[n] \times s[n] \tag{9}$$

i.e. $p_I[n] =$

$$\begin{cases} 32767 \times \left(A_{dc} + G \sin \left(2\pi \pi \left(\frac{10}{500} \right) + \Phi \right) \right) \sin \left(2\pi \pi \left(\frac{10}{500} \right) \right) & 0 \leq n \leq 199 \\ 0 & \text{else } n \end{cases} \tag{10}$$

$$p_Q[n] = y_{\text{RefCos}}[n] \times s_{\text{wind}}[n] \tag{11}$$

i.e. $p_Q[n] =$

$$\begin{cases} 32767 \times \left(A_{dc} + G \sin \left(2\pi \pi \left(\frac{10}{500} \right) + \Phi \right) \right) \cos \left(2\pi \pi \left(\frac{10}{500} \right) \right) & 0 \leq n \leq 199 \\ 0 & \text{else } n \end{cases} \tag{12}$$

Figure 2 shows the magnitude frequency spectrum of $p_I[n]$, which is a result of the frequency-domain periodic convolution between the spectra of $y_{\text{RefSine}}[n]$ and $s[n]$. Similarly, figure 3 shows the magnitude frequency spectrum of $p_Q[n]$, which is a result of the frequency-domain periodic convolution between the spectra of $y_{\text{RefCos}}[n]$ and $s[n]$.

The final summation sub-processes of equations 3 and 4 can be explained as follows [19, 20]. The L-point Discrete Fourier Transform (DFT) [18] of the signal $p_I[n]$ (of

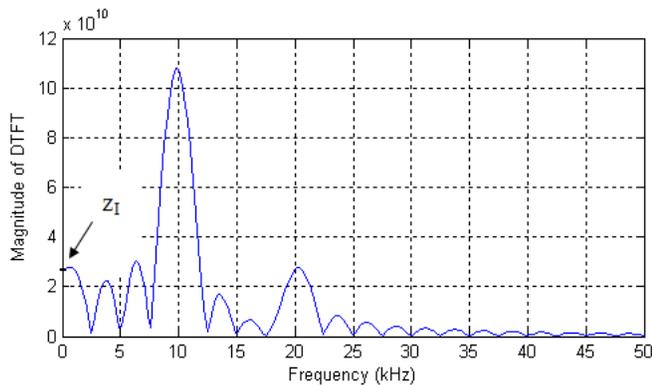


Fig. 2 Magnitude frequency spectrum of $p_I[n]$; magnified portion up to 50 kHz is shown

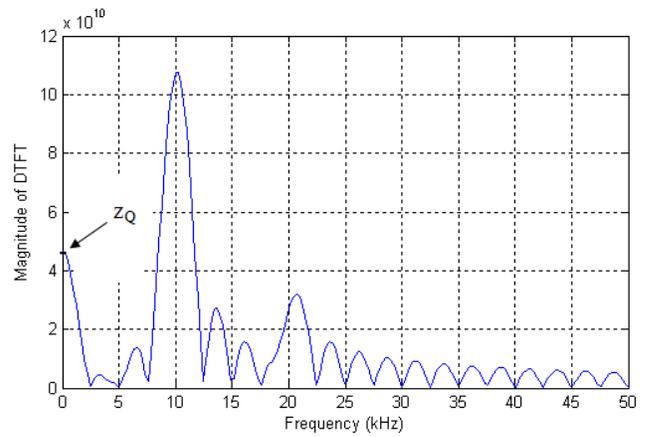


Fig. 3 Magnitude frequency spectrum of $p_Q[n]$; magnified portion up to 50 kHz is shown

equation 9) can be calculated as

$$P_I[k] = \sum_{n=0}^{L-1} p_I[n] \cdot e^{-j2\pi kn / L} \tag{13}$$

Equation 13 reduces to equation 3 for $k=0$, suggesting that equation 3 is calculating zero frequency component of the L-point DFT of $p_I[n]$. Thus the amplitude of the zero-frequency component in the plot of figure 2, viz. 2.6843×10^{10} , is the final PSD result of the I-arm z_I of equation 3. Similarly, equation 4 is calculating zero frequency component of the L-point DFT of the signal $p_Q[n]$ (of equation 11). Consequently, the amplitude of the zero-frequency component in the plot of figure 3, viz. 4.6493×10^{10} , is the final PSD result of the Q-arm z_Q of equation 4.

2.1 Interpretation using Accumulator-Sampler

Another, new, interpretation of the final summation sub-process of equations 3 and 4 is that the summer is equivalent to an accumulator-sampler cascade. Its operation can be explained in time- and frequency-domains separately.

2.1.1 Time-domain interpretation of

Accumulator-Sampler:

The input to the L-point accumulator is the signal $p_I[n]$. The output of the accumulator $p_{I\text{acc}}[n]$ is the time-domain convolution (equation 14) of $p_I[n]$ and $h[n]$. The function $h[n]$ is the impulse response of accumulator, which is a rectangular pulse of L samples having unity amplitudes.

$$p_{I\text{acc}}[n] = \sum_{k=0}^{L-1} p_I[k] \cdot h[n-k] \tag{14}$$

Figure 4 shows the output signal of the accumulator $p_{I\text{acc}}[n]$, comprising $2L-1$ samples. The next stage of sampler picks only one sample of $p_{I\text{acc}}[n]$. It is that sample of the convolution result when both functions $p_I[n]$ and $h[n]$ in their convolution operation are fully overlapping. This happens when $n = L-1$ in equation 14, which then becomes equation 3. Thus the output of the sampler is the sample number $L-1=199$ of $p_{I\text{acc}}[n]$; this is the final PSD result of the I-arm viz. $z_I = 2.6843 \times 10^{10}$, as shown in figure 4. It is relevant to mention here that equation 3 can also be

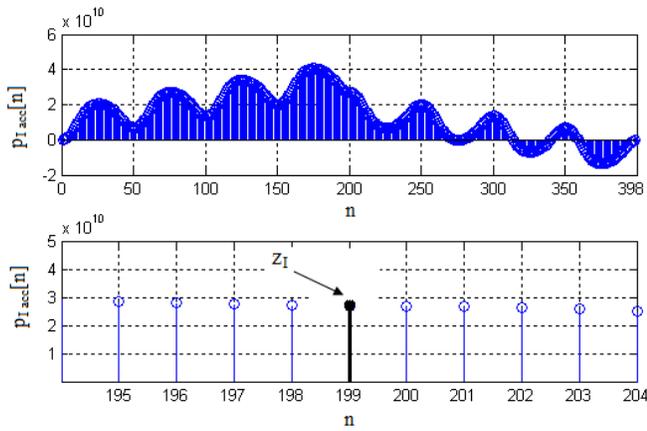


Fig. 4 Time-domain plot of the accumulator output signal $p_{iacc}[n]$ in two timescale ranges

interpreted as implementing the digital matched filtering, as the signal $y_{RefSine}[n]$ comprises 4, i.e. integer, no. of cycles; thus $y_{RefSine}[n]$ can also be considered as the impulse response of the filter matched with the measured signal $s[n]$.

2.1.2 Frequency-domain interpretation of Accumulator-Sampler:

The output of the accumulator in frequency-domain (figure 5) is a result of multiplication of the magnitude frequency spectrum of the input $p_i[n]$ (figure 2) and magnitude frequency response of the accumulator. The accumulator part is followed by the sampler part, which extracts the zero-frequency component of this product, yielding the single number z_I as the PSD result. Similarly considering the quadrature-phased PSD calculation, the same time- and frequency-domain interpretations can be given for equation 4, using figures 6 and 7.

These figures show the output signal of the accumulator $p_{Qacc}[n]$ in time- and frequency-domain respectively.

The magnitude frequency response of the accumulator has nulls at the integer multiples of 2.5 kHz, which is the ratio of the signal frequency (10 kHz) and the integer number of cycles (4) of the measured signal [6] being used in the PSD. This choice of an integer number of cycles of the measured

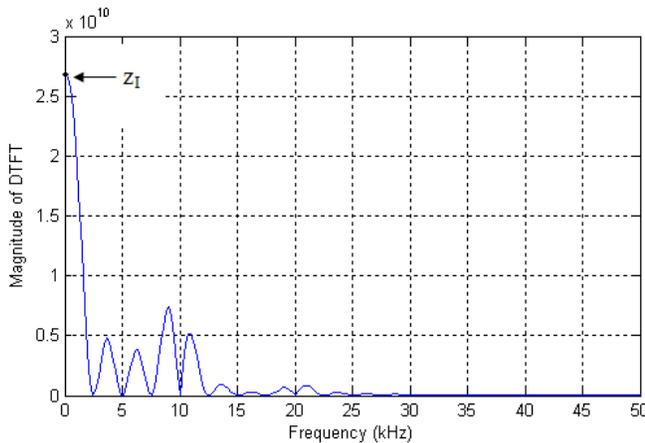


Fig. 5 Magnitude frequency spectrum of the accumulator output signal $p_{iacc}[n]$; magnified portion up to 50 kHz is shown

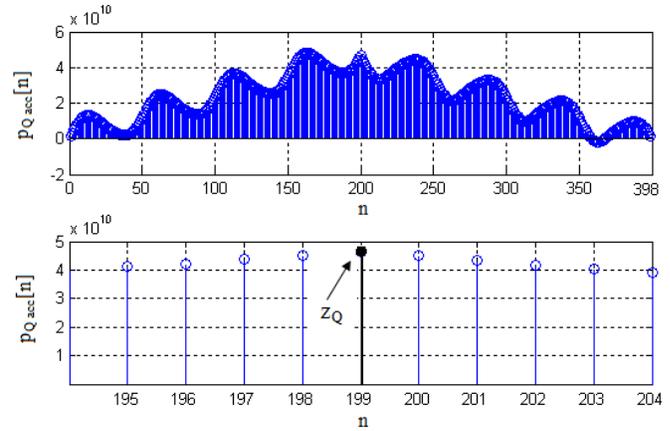


Fig. 6 Time-domain plot of the accumulator output signal $p_{Qacc}[n]$ in two timescale ranges

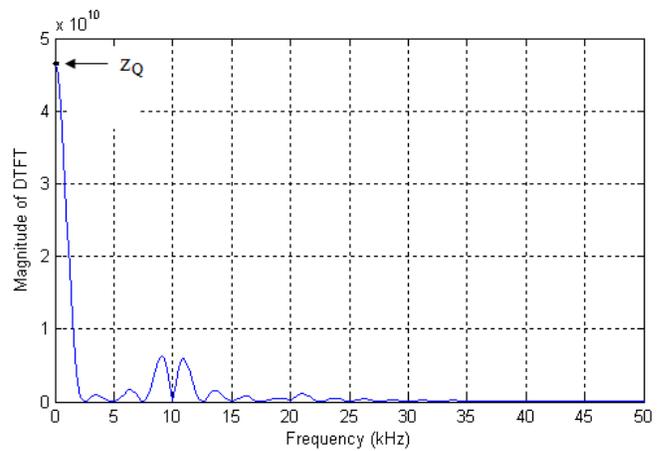


Fig. 7 Magnitude frequency spectrum of the accumulator output signal $p_{Qacc}[n]$; magnified portion up to 50 kHz is shown

signal for use in the PSD calculation thus ensures that the PSD reference signal has no dc component, which if present would invalidate the PSD calculations.

The accuracy of the final PSD results can be checked against the known amplitude and phase values of the unipolar signal. Based on equations 1 and 2, the amplitude (A) and phase (ϕ) values of the measured unipolar signal can be calculated as follows:

$$A = \frac{2 \times \sqrt{z_I^2 + z_Q^2}}{KB} \quad (15)$$

$$\phi = \tan^{-1} \frac{z_Q}{z_I} \quad (16)$$

K is the product of the overall conversion factor as the phase- and dc-level-shifted sinusoidal signal ($s[n]$ of equation 7) is processed through the various sub-stages of PSD operation. In this Matlab-based example, the value of K is simply L, i.e. the number of samples used in the PSD operation. In a hardware-implemented system, K would be a

product of L and various other gain/conversion factors as the signal is processed through the system (see section 3.2).

Using z_i , z_0 , K and B as 2.6843×10^{10} , 4.6493×10^{10} , 200 and 32767 respectively in equation 15 yields $A = 16384$, which is equal to G, i.e. the amplitude of the example signal $s[n]$. Similarly, equation 16 gives $\phi = \pi/3$ which is equal to the original phase shift Φ in $s[n]$.

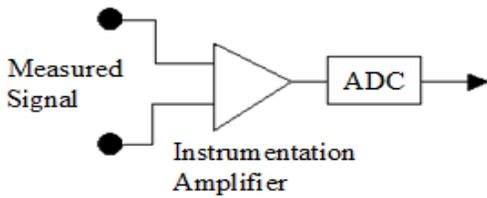


Fig. 8 Schematic diagram of the set-up, which gives input samples to the PSD system of the voltage measurement channel

3. TWO IMPORTANT ISSUES

IN DIGITAL IMPLEMENTATION OF PSD

In the design and implementation of the FPGA-based digital PSD system, following two aspects were important in relation to the precision of the final PSD result.

3.1 Number of waveform samples used in digital PSD calculation

In an ADC-based digital measurement system (figure 8), the overall SNR (in dB) of the measurement stage can be described as [21]

$$SNR = 6.02B + 1.76 + 20\log(FFS) + 10\log\left(\frac{f_s/2}{BW}\right) \quad (17)$$

where: B = ADC resolution in bits (16 in the system presented here)

FFS = fraction of the full-scale range of the ADC being used (1 here)

f_s = ADC sampling rate (500 kHz here)

$f_s/2$ is the Nyquist frequency of the ADC sampling process

BW = Bandwidth of the final output

The last term in equation 17 (the ratio Nyquist frequency/bandwidth) has been called “process gain” by Kester & Bryant [21] and is critical. Till the output of the ADC, this factor has zero value, i.e. log of unity, as the occupied bandwidth of the signal, set by the anti-aliasing filter, is the same as the Nyquist frequency $f_s/2$. However, the process gain increases after the PSD process. This is because the bandwidth of the signal after the PSD process is reduced, in inverse relationship with the number of samples L used in the PSD process, as discussed in section 3. Thus, every quadrupling in L results in the quadrupling of the ratio Nyquist frequency/bandwidth, and consequently in an increase of 6.02 dB in SQNR, i.e. an improvement of 1 bit in effective bit resolution [2, 6]. Thus, the factor of “process gain” contributing to the overall SNR of the measurement system is directly dependent on the number of samples L used in the PSD process.

The fact that every quadrupling in L results in an increase of 6.02 dB in the overall SNR was tested practically by developing two different versions of the FPGA firmware to implement the PSD operation on 1 and 4 cycles of the measured sinusoid. The final measurements showed an improvement of almost 5 dB in the achieved SNR when 200 samples from 4 cycles, instead of 1 cycle having 50 samples, were used. Hence for final implementation of the FPGA-based PSD system, L was selected as 200.

3.2 Finite word length effect on PSD Precision

In dsp implementations, increase in the number of bits required to store the results of addition and multiplication operations must be controlled. This increase means more cost and, in an FPGA, more usage of FPGA resources, resulting in higher power consumption. On the other hand, the usage of a finite number of bits for the results of dsp calculation introduces other errors. These errors can be of overflow, round-off or truncation types, and have been given various names in dsp literature like finite word-length / register-length effect, bit-resolution effect or dsp noise [22]. The remedy is to use sufficiently long words to store results.

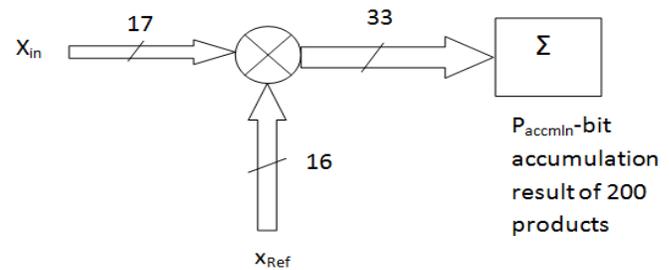


Fig. 9 Bit growth in PSD calculation, in I or Q arm of one measurement channel

In the FPGA-implemented PSD system presented here, there are various stages where usage of a finite number of bits would potentially result in finite word length errors. A careful analysis was required to assess the optimal number of bits to be used. Figure 9 shows the block diagram of the I or Q arm of the PSD algorithm, as implemented in each of the 35 measurement channels in the ‘Xtreme DSP’ slice of the Virtex-4 SX35 FPGA, along with the bit-resolutions actually used. In this figure, X_{in} is the measured unipolar sinusoidal signal coming from the 16-bit ADC, while X_{Ref} is the reference sinusoid coming from the look up table. As each Xtreme DSP slice comprises an 18 x 18 multiplier, an adder and a 48-bit accumulator [23], the need for the 17x16 multiplication, taking place in the PSD module, is provided for. No product needs to be rounded off and hence there is no round-off error before the accumulation stage.

The number of bits (P_{accmln}) allocated for storing the final accumulation result of PSD required careful evaluation. This evaluation would tell whether the 48 bit accumulator in the Xtreme DSP slice is sufficient. It was also very important that P_{accmln} should not be much more than the actual requirement, since only the 16 most significant bits had to be picked out of the accumulator, as per the system specs. This

meant that the final $V_{out,I}$ and $V_{out,Q}$ results would effectively be the accumulation result divided by $2^{P_{accmln}-16}$. In order to keep the SQNR of these final results above 80 dB, the value of P_{accmln} had to be such that the result after this division would occupy at least 14 bits, giving 86 dB SQNR. In such a case, the accumulation result would occupy $P_{accmln}-1$ or $P_{accmln}-2$ bits.

Here is how the value of P_{accmln} was evaluated. The PSD operation took place over 200 samples; hence the accumulation result of 200 products (each having bit resolution of 33 bits) would occupy $P_{accmln} = 33 + \Delta P$ bits. If the two signals being multiplied in the PSD calculation had been occupying the full dynamic range of 16-bits in *all* of their samples, e.g. considering both signals as square-wave, the value of ΔP would be $\log_2(200)=7.64$ bits. However, as both of the signals being multiplied are sinusoids, not square-waves, ΔP would be less than 7.64. This meant that P_{accmln} could be expected to be around or less than 40 bits.

The final selection of P_{accmln} was done empirically. Three different PSD firmware versions, having P_{accmln} of 39, 38 and 37, were used for measurement, and the captured data was analysed to assess the occupation range of the calculated $V_{out,I}$ and $V_{out,Q}$ values. With reference to equation 15 (where $K = 10.2$, being a product of L and three other gain/conversion factors as the signal was processed through the digital measurement system, *viz.* conversion factor between ADC input and output, gain of the instrumentation amplifier used and scaling factor due to bit truncation when picking 16 MSBs out of P_{accmln}), the value of precision in the measurement was 5.97, 11.93 and 23.87 μV , for $P_{accmln} = 37, 38$ and 39 bits respectively. These precision values are visible in figure 10 (a), (b) and (c).

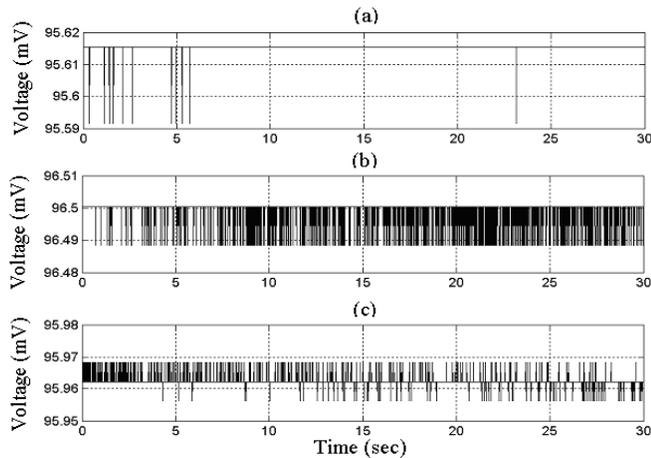


Fig. 10 Signal measured using firmware versions having $P_{accmln} =$ (a) 39 (b) 38 (c) 37 bits

More experiments were conducted with these three PSD firmwares to assess the amount of various types of noise present in the measured voltages and the role of the selected P_{accmln} in this regard. Finally, P_{accmln} was decided to be set at 38-bit. With this value of P_{accmln} , there would not be an overflow error in the accumulation result, as the accumulator size in the 'Xtreme DSP' slice is 48-bit. The only source of

error in the accumulation result would be the picking of 16 MSBs from the P_{accmln} -bit result, i.e. truncation error.

4. PSD SYSTEM DEVELOPMENT AND IMPLEMENTATION

This digital PSD system is incorporated in the 35 parallel voltage-measurement channels of the EIT instrument fEITER, through the firmware loaded on the Xilinx Virtex-4 SX35 FPGA [11, 24]. On the measurement side, the measured EIT voltages, for each of the 35 channels, are sampled by the 16-bit unipolar ADC at 500 kS/s, providing 50 samples for each of the 5 cycles of the injected current. The PSD module implements PSD process over last 4 cycles, i.e. 200 samples, of every new current injection; first cycle is let pass for current settling. A look-up table comprising 200 samples is used for each of the two, in-phase and quadrature-phase, reference signals in the PSD module.

The PSD code was first developed in Matlab and fine-tuned using Matlab-generated sinusoids of different frequencies, phase-shift and amplitude. After finalisation of the code, its VHDL version was developed and incorporated in the full system firmware. The number of bits allocated to the final PSD result in the VHDL code required careful selection, as explained above in section 3. To verify the final in-phase and quadrature values, $V_{out,I}$ and $V_{out,Q}$, obtained from the PSD calculations, various test-vectors were pasted in the VHDL code to act as input signals, the test vectors having already been verified in Matlab simulation.

Usage of FPGA Resources

Approximately 40 % of the 15360 slices of the Virtex-4 SX35 FPGA are taken by the 35 channel PSD module. Some usage of these slices occurs in the two look up tables, of 200 samples each, of the PSD reference signals. These 400 samples are stored in 400 16-bit registers; thus only this storage takes up 400 i.e. 2.6 % slices. Further logic resources are used for connecting these registers to all of the 35 PSD channels. The core of the PSD calculation, *viz.* the multiply-accumulate operation, is implemented in 70 of the 'XtremeDSP' slices available in the Xilinx Virtex-4 SX35 FPGA, as two DSP-slices implement the multiply-accumulate arms of I and Q demodulation separately, for each of the 35 channels.

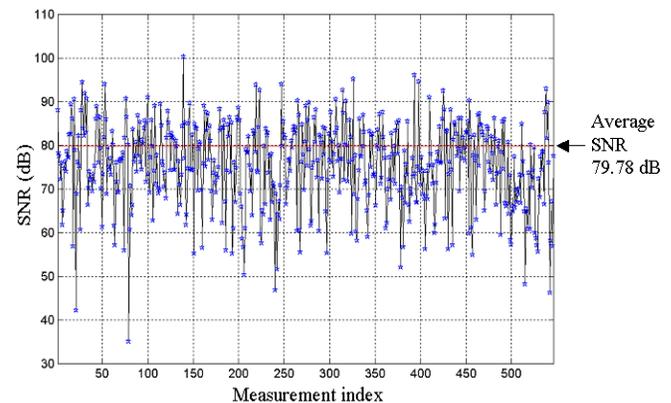


Fig. 11 SNR for each of 546 measurements, calculated over 500 EIT frames

5. EIT INSTRUMENT TESTS AND RESULTS

As is the routine for testing of EIT instruments, tank tests were conducted to assess the overall instrument's performance, with the above mentioned PSD firmware incorporated in the complete fEITER system. Results for some early and numerous later-conducted tests were reported in [25, 26] and [27] respectively. These tests mainly used cylindrical and head-like tanks containing a homogeneous saline solution of (typical) conductivity 500 $\mu\text{S}/\text{cm}$, through which polar current injection patterns were passed. In one example of head-like phantom tests with homogeneous saline solution, differential voltage measurements on adjacent electrodes displayed typical SNR values near 80 dB, with some reaching 90 dB and beyond (Figure 11).

For two different experiments with reference saline solutions, two plots of in-phase voltage components ($V_{\text{out},i}$) measured on one of the channels are shown in figure 12. As explained in section 3.2 above, firmware with $P_{\text{acmln}} = 38$ bits was used. (The consequent 12 μV measurement precision, i.e. the variation over 1 code, is visible in the plots.) The measurements shown range over, not 1 but, 4-5 codes. Thus the dominant noise in these measurements is not quantisation noise. Rather it is the noise contributed by other sources like external pick up, disturbance in the subject medium and intrinsic noise in the analogue electronics.

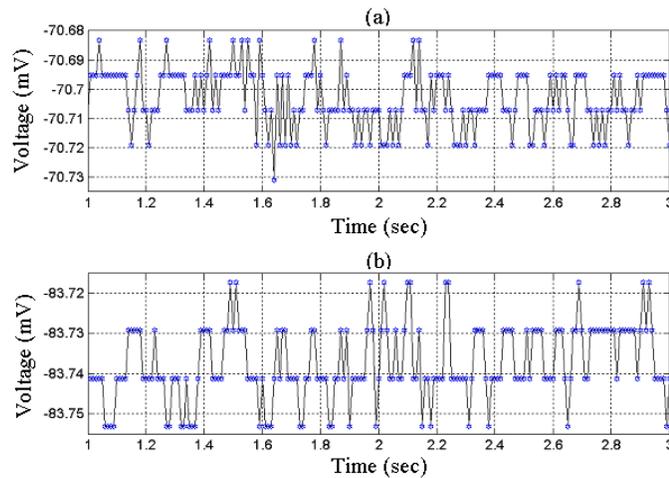


Fig. 12 In-phase components measured for reference saline solution in two different experiments, with $P_{\text{acmln}} = 38$ -bit

This other noise is well above the level of the quantisation noise determined by $P_{\text{acmln}} = 38$ bits.

Continuing with the tank tests, various objects such as metallic or insulating rods, or sponges prepared in solutions of various conductivities, were placed in the baseline solution to introduce inhomogeneity during EIT data capture. These resulted in changes in measured voltages, from pre- to post-perturbation condition, due to the changes in the conductivity and/or permittivity of the medium inside the tank. For one such experiment, Figure 13(a) shows the plot of absolute changes in voltage magnitudes for all EIT measurement indices (i.e. combinations of the two separate pairs of electrodes, used for current injection and voltage

measurement). One of these measurement indices, viz. no. 166, corresponding to current injection at electrode pair 7-15 and voltage measurement at electrode pair 11-12, has got a relatively low value of voltage change viz. 44.9 μV (shown as red-coloured in the plot of figure 13(a)). Figure 13(b) shows its time-based plot, over one minute, of the voltage magnitudes. This plot shows that it is nearing the noise limit, with the measured change in voltage magnitude slightly higher than the noise level. The plot still shows a well-resolved change of 0.162 %. This is the typical case of having 'detectable' and 'non-detectable' voltage changes. The signal shown in figure 13(b) is still detectable. But for those measurement indices in figure 13(a) having smaller voltage values, the signal changes would not be detectable as these will be buried in noise. This type of test explores the capability of the EIT instrument to resolve inhomogeneities of very small spatial extent, though of high conductivity contrast. Results of these and similar other tests demonstrated the fEITER system's measurement capability to resolve easily the cases where large conductivity changes occur over very small spatial regions within the subject.

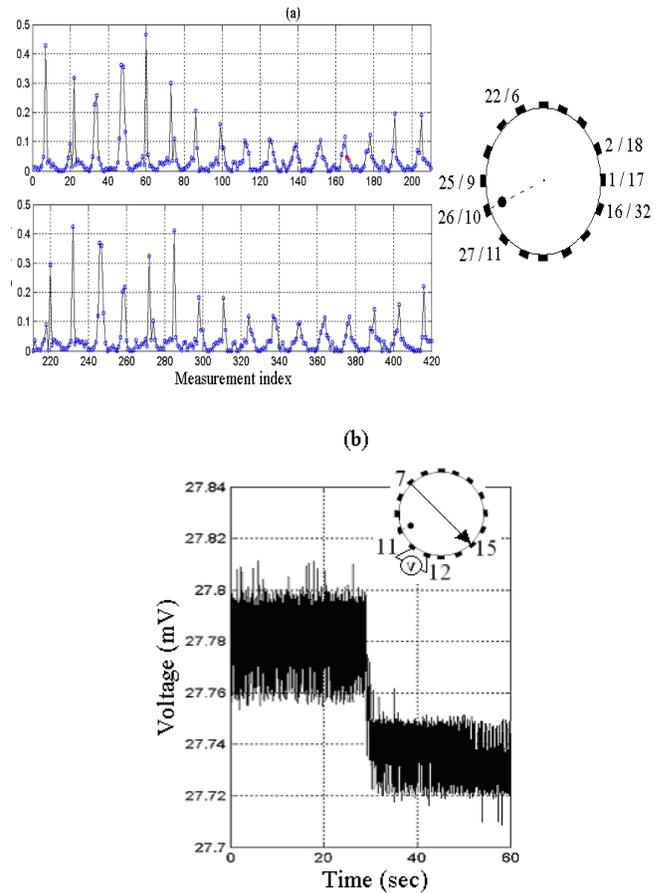


Fig. 13 (a) Absolute change in voltage magnitude, pre- and post-insertion of wooden rod in saline-filled tank (b) Time-based plot of voltage magnitudes for the measurement index no. 166 of (a) (shown as red-coloured)

Test results using precision resistor wheel have been reported in [11]. Results of hospital tests on humans have been reported in [11, 24, 28, 29, 30].

6. CONCLUSION

This paper presents a digital PSD system implemented in FPGA, which is incorporated in a multi-channel bio-medical EIT instrument. In the paper, first a Matlab-based case of digital PSD has been analyzed using time- and frequency-domain methods of signal processing theory and a new interpretation of digital PSD in terms of accumulator-sampler has been given. The simulated signal used therein is similar to the measured signal of the practically-implemented FPGA-based system. Then the design and implementation of the FPGA-based digital PSD system has been discussed. Two important issues, viz. number of digitized waveform samples for use in PSD calculation and number of bits allocated for storage of digital results, have been explored, both of which ultimately affect the precision of the final PSD result. The analysis to evaluate the number of bits required for storing the final accumulation result of PSD has been presented. Consequently, there is truncation error in the final PSD result, but no overflow or round-off errors. The implemented 35-channel PSD system uses 40 % slices of the Xilinx Viretx-4 SX35 FPGA, along with 70 'Xtreme DSP slices'. Tank test results of the EIT instrument fEITER incorporating this digital PSD system have shown good noise performance, achieving an overall SNR of almost 80 dB, at the high data-capturing rate of 100 frames/sec. The results have also demonstrated the instrument's measurement capability to resolve easily the cases where large conductivity changes occur over very small spatial regions within the subject.

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ABBREVIATIONS USED

ADC: Analogue-to-digital converter;
 DFT: Discrete Fourier Transform;
 DTFT: Discrete-time Fourier Transform;
 DSP: Digital signal processor;
 dsp: Digital signal processing;
 EIT: Electrical impedance tomography;
 fEITER: Functional Electrical Impedance Tomography of Evoked Responses;
 FPGA: Field Programmable Gate Array;
 MSB: Most significant bit
 PSD: Phase-sensitive detection;
 SNR: Signal-to-noise ratio;
 SQNR: Signal to quantization noise ratio;
 VHDL: VHSIC Hardware Description Language.

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